RAKESH KUMAR

Contact Information

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Research Interests

- **Broad:** Computer architecture with aspects of VLSI design and code generation/optimization.
- **Current focus:** Server processor architecture, Memory hierarchy for emerging memory technologies.

Education

- **Doctor of Philosophy:** Computer Architecture   **July 2014**
  Universitat Politècnica de Catalunya (UPC), Barcelona, Spain.
  Advisors: Prof. Antonio González, Dr. Alejandro Martínez.
  Thesis: Optimizing SIMD Execution in HW/SW Co-designed Processors.

- **Master of Engineering:** Microelectronics   **Dec 2008**
  Birla Institute of Technology and Science (BITS), Pilani, India (*CGPA: 10/10*).
  Advisor: Prof. TSB Sudarshan
  Thesis: Cache Design issues in Multi-core Architectures

- **Bachelor of Technology:** Electronics & Communication Engineering   **July 2005**
  Kuruksherta University, Kurukshetra, India (*First Division with Honours*)

Work Experience

- **Associate Professor,** *NTNU*   **June 2018 – Present**
- **Postdoctoral Researcher,** *Uppsala University*   **Aug 2017 – May 2018**
  - Investigated energy-efficient processor core designs.
- **Postdoctoral Research Associate**, *University of Edinburgh*   **Jan 2015 – June 2017**
  - Specialized microarchitecture and memory hierarchy for server processors.
- **Graduate Intern Researcher**, *Intel Barcelona Research Center, Intel Labs*   **Oct 2013-May 2014**
  - Developed memory controllers for Intel Skylake server architecture.
  - Received Intel Spontaneous Level II/Excellence Award.
- **Assistant Lecturer**, *BITS, Pilani, India*   **Jan 2009-July 2009**
  - Co-taught a course on Microprocessor Programming and Interfacing to a class of 250+ students.
- **Graduate Engineer Trainee**, *Himachal Futuristic Communication Ltd., India*   **July 2005-July 2006**

Awards and Grants

- Four Hipeac Paper Awards for papers published at HPCA'19, ASPLOS'18, HPCA'17, and MICRO'16.
- Mehdi Alipour (my co-advisee) got runner-up award in Student Research Competition at MICRO'18.
- Intel Spontaneous Level II/Excellence Award in 2014 for work on memory controllers.
- Recipient of FPI-UPC grant for PhD (Jan 2010 – Oct 2013).
- Student travel grant to attend HiPC-2008 in Bangalore, India.
- Best Presentation Award for "Adaptive Block Pinning for Multi-core Architectures" at HiPC-SS08.
- Best Paper Award for "Non Inclusion Property in Multi Core Architectures with Multi-level Caches" at National Conference on High Computing Technologies, India, Nov 2008.

Selected Talks

- Blasting Through The Frontend Bottleneck With Shotgun
  - ARM Research Summit, Cambridge, UK.   **September 2018**

- Boomerang: Metadata-Free Control Flow Delivery for Servers
  - ARM Research Summit, Cambridge, UK.   **September 2017**

- Tailoring Server Architectures to Application Demands
  - ETH Zurich, Switzerland.   **March 2017**
  - Queen's University Belfast, UK.   **February 2017**
  - Uppsala University, Sweden.   **November 2016**

- Optimizing SIMD Execution in HW/SW Co-designed Processors.
  - Amrita School of Engineering, Bangalore, India.   **March 2015**

Professional Services

- **Program Committee**
  - International Parallel and Distributed Processing Symposium (**IPDPS**) *[2019]*
  - International Conference on Parallel Processing (**ICPP**) *[2017]*
  - Nordic Workshop on Multi-Core Computing (**MCC**) *[2017]*
- **External Review Committee**
  - International Symposium on High Performance Computer Architecture (**HPCA**) *[2019]*
- **Conference Review** (Not PC/ERC):
  - International Symposium on High Performance Computer Architecture (**HPCA**) *[2017, 2016, 2013]*
  - International Symposium on Workload Characterization (**IISWC**) *[2017]*
  - International Conference on Code Generation and Optimizations (**CGO**) *[2016]*
  - International Conference for High Performance Computing, Networking, Storage and Analysis (**SC**) *[2016]*
  - International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**) *[2015]*
  - International Symposium on Computer Architecture (**ISCA**) *[2015]*
- **Journal Review**
  - IEEE Transactions on Computers (TC).
  - IEEE Computer Architecture Letters (CAL).
  - Technical Gazette.
- **Software**
  - Co-developer of DARCO, the first academic simulation infrastructure for research on HW/SW co-designed Virtual Machines.

Supervision

- **PhD Students**
  - Truls Asheim, *NTNU*   **2019 - Present**
  - Mehdi Alipour, *Uppsala University* [Co-supervising with Prof. David Black-Schaffer]   **2017 - Present**
- **Masters Students**
  - Gem Dot, *UPC Barcelona* [Mentored with Prof. Antonio Gonzalez]   **Spring 2012**
    Thesis: Efficient Emulation of x86 ISA in Co-designed Virtual Machines.

Teaching

- **NTNU, Norway**
  - Embedded System Design Project *(TFE-4208)*   **Spring 2019**
  - Low-Level Programming *(TDT-4258)*   **Fall 2018**
  - Architecture of Computing Systems *(TDT-01)*   **Fall 2018**
- **Uppsala University, Sweden**
  - Parallel Programming for Efficiency   **Fall 2017**

- **University of Edinburgh, UK**
  - Computer Architecture *(Roles: Teaching Assistant, Guest Lecturer)* **Spring 2016**
  - Introduction to Computer Systems *(Roles: Teaching Assistant, Guest Lecturer)* **Fall 2015, 2016**
- **Birla Institute of Technology and Science (BITS) Pilani, India** **2007-2009**
  - Microprocessor Programming and Interfacing. *(Role: Guest Lecturer)*
  - Digital Electronics and Microprocessors. *(Role: Teaching Assistant)*
  - Microelectronics Circuits. *(Role: Teaching Assistant)*
  - Electronics Devices and Integrated Circuits. *(Role: Teaching Assistant)*

Pedagogical Training

- University of Edinburgh
  - *Handling International Students' Writing Problems.* **March 2017**
  - *Tutoring and demonstrating – Tricks and Challenges.* **Feb 2016**
- Birla Institute of Technology and Science (BITS) Pilani, India
  - *Intensive Teaching Workshop.* **Spring 2009**

Publications

Peer-reviewed Journals

- **Assisting Static Compiler Vectorization with a Speculative Dynamic Vectorizer in a HW/SW Co-designed Environment.**
  R. Kumar, A. Martínez, and A. González. In ACM Transactions on Computer Systems (**ACM TOCS**), Volume 33 Issue 4, Article 12, January 2016.

- **Efficient Power Gating of SIMD Accelerators through Dynamic Selective Devectorization in a HW/SW Co-designed Environment.**
  R. Kumar, A. Martínez, and A. González. In ACM Transactions on Architecture and Code Optimization (**ACM TACO**), Volume 11 Issue 3, October 2014.

Peer-reviewed Conferences

- **Freeway: Maximizing MLP for Slice-Out-of-Order Execution.**
  R. Kumar, M. Alipour, and D. Black-Schaffer. In International Symposium on High Performance Computer Architecture (**HPCA**), 2019.

- **FIFOrder MicroArchitecture: Ready-Aware Instruction Scheduling for OoO Processors.**
  M. Alipour, R. Kumar, S. Kaxiras, and D. Black-Schaffer. In Design, Automation and Test in Europe Conference and Exhibition (**DATE**), 2019.

- **Blasting Through The Front-End Bottleneck With Shotgun.**
  R. Kumar, B. Grot, and V. Nagarajan. In International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), 2018.

- **HW/SW Co-designed Processors: Challenges, Design Choices and a Simulation Infrastructure for Evaluation.**
  R. Kumar, J. Cano, A. Brankovic, D. Pavlou, K. Stavrou, E. Gibert, A. Martinez, and A. Gonzalez. In IEEE International Symposium on Performance Analysis of Systems and Software (**ISPASS**) 2017.

- **Boomerang: A Metadata-free Architecture for Control Flow Delivery.**
  R. Kumar, C. Huang, B. Grot, and V. Nagarajan. In International Symposium on High Performance Computer Architecture (**HPCA**), February 2017.

- **C3D: Mitigating the NUMA Bottleneck via Coherent DRAM Caches.**
  C. Huang, R. Kumar, M. Elver, B. Grot, and V. Nagarajan. In International Symposium on Microarchitecture (**MICRO**), October 2016.

- **Quantitative Characterization of the Software Layer of a HW/SW Co-designed Processor.**
  J. Reyes, R. Kumar, A. Brankovic, D. Pavlou, K. Stavrou, E. Gibert, A. Martinez, and A. Gonzalez. In International Symposium on Workload Characterization **(IISWC)**, September 2016.

- **Speculative Dynamic Vectorization to Assist Static Vectorization in a HW/SW Co-designed Environment.**
  R. Kumar, A. Martínez, and A. González. In International Conference on High Performance Computing **(HiPC)**, December 2013.

- **Vectorizing for Wider Vector Units in a HW/SW Co-designed Environment**.
  R. Kumar, A. Martínez, and A. González. In International Conference on High Performance Computing and Communications **(HPCC)**, November 2013.

- **Dynamic Selective Devectorization for Efficient Power Gating of SIMD units in a HW/SW Co-designed Environment.**
  R. Kumar, A. Martínez, and A. González. In International Symposium on Computer Architecture and High Performance Computing **(SBAC-PAD)**, October 2013.

- **Speculative Dynamic Vectorization for HW/SW Co-designed Processors.**
  R. Kumar, A. Martínez, and A. González. In International Conference on Parallel Architectures and Compilation Techniques **(PACT)**, September 2012. (Short Paper)

Peer-reviewed Workshops/National Conferences:

- **Minimum Out-of-Order Core.**
  M. Alipour, R. Kumar, S. Kaxiras, and D. Black-Schaffer. In Student Research Competition held at 51st Annual IEEE/ACM International Symposium on Microarchitecture **(MICRO)** 2018. [*Best Student Poster* runner-up]

- **DARCO: Infrastructure for Research on HW/SW co-designed Virtual Machines.**
  D. Pavlou, A. Brankovic, R. Kumar, M. Gregori, K. Stavrou, E. Gibert, and A. Gonzalez. In Proceedings of the 4th Workshop on Architectural and Microarchitectural Support for Binary Translation **(AMAS-BT)**, held in conjuction with the 38th International Symposium on Computer Architecture **(ISCA)**, June 2011.

- **Adaptive Block Pinning for Multi-core Architectures.**
  R. Kumar, N. Chaturvedi, and TSB Sudarshan. In the web proceedings of 15th International Conference on High Performance Computing, student symposium **(HiPC-SS08)**, December 2008. [*Best Presentation Award*]

Non-Peer Reviewed Conferences and Workshops:

- **Speculative Dynamic Vectorization to Assist Static Vectorization in a HW/SW Co-designed Environment.**
  R. Kumar, A. Martínez, and A. González. In Hipeac Compiler, Architecture and Tools Conference at Haifa, Israel, November 2013.

- **Modelling HW/SW Co-Designed Processors.**
  J. Cano, A. Brankovic, R. Kumar, D. Zivanovic, D. Pavlou, K. Stavrou, E. Gibert, A. Martínez, G. Dot, F. Latorre, A. Barceló, and A. González. In Eighth International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems **(ACACES)**, July 2012.

- **Non Inclusion Property in Multi Core Architectures with Multi-level Caches.**
  R. Kumar, N. Chaturvedi, and TSB Sudarshan. In the proceedings of National Conference on High Computing Technologies, November 2008, India. [*Best Paper Award*]

Languages

English – Full Proficiency
Spanish – Working Proficiency
Hindi – Native