CURRICULUM VITAE

Short biography

Per Gunnar Kjeldsberg was born in Trondheim, Norway in 1966. He received his Sivilingeniør degree (MSc) in electrical engineering in 1992 from the Norwegian Institute of Technology (NTH). In 2001 he received the degree of Doktor ingeniør (PhD) from the same institution (now Norwegian University of Science and Technology, NTNU). Between 1992 and 1996 he worked as a design engineer at the company Eidsvoll Electronics AS. Kjeldsberg is currently Professor at Department of Electronic Systems, NTNU. His research interests are energy efficient embedded computing systems, with a focus on Internet of Things and digital signal processing applications. He has participated in several national and international research projects and is member of the European Network of Excellence HiPEAC. He was work package leader of the EU Horizon 2020 FET-HPC project READEX (2015-208) and principal researcher in the LEIT project Tulipp (2016-2019). Currently he is supervisor in the MSCA-IF project Palmera. At NTNU Kjeldsberg has been group leader of the Circuit and Radio Systems group and project leader for a strategic research initiative on Energy Efficient Computing Systems, one of seven groups selected to receive special support towards EU's research program Horizon 2020. Throughout his career, Kjeldsberg has cooperated closely with imec, in Leuven, Belgium, where he has been visiting researcher for nine months in all. He has also been visiting researcher at University of California, Irvine, Center for Embedded Computer Systems, at imec Netherlands at the Holst Centre in Eindhoven, and is currently on a one year research stay at School of Computer Science and Engineering, University of New South Wales, Sydney, Australia. Kjeldsberg has published extensively at conferences and in journals and has been coauthor of three books in his fields of interest. At NTNU he teaches both undergraduate and graduate courses, and supervises students at master, PhD, and post.doc level. Kjeldsberg is and has been a member of the board of directors both at the Faculty and in private companies. He is frequently used as reviewer for several international journals and conferences.

Personal Information

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Formal Education

1996-2001:	Doktor Ingeniør (Ph.D., electrical engineering) from the Norwegian University of Science and Technology
1987-1992:	Sivilingeniør (graduate degree in electrical engineering, microelectronics) from the Norwegian Institute of Technology (now part of NTNU)

Employment

2007 – Present:	Professor at Department of Electronics and Telecommunications / Department of Electronics Systems, NTNU
2002 – 2007:	Associate Professor at Department of Physical Electronics / Department of Electronics and Telecommunications, NTNU
2001:	Associate Professor / Post.doc at Department of Physical Electronics, NTNU
1992-1996:	Design Engineer at Eidsvoll Electronics AS
1988, 89, 91:	Summer employment at Telenor Research and Development
1986-1987:	Norwegian Army, trained to be and practicing as a sergeant

Current Projects and Responsibilities

- Supervisor of post.doc Azam Seyedi in the Horizon 2020 Marie Skłodowska-Curie Individual Fellowships project PALMERA (Low Power and Fault Tolerant Cache Memory Design through a Combination of Hardware and Software Approaches).
- Member of the HiPEAC (High-Performance and Embedded Architecture and Compilation) European Network of Excellence (Seventh Framework Program).
- Member of the interdepartmental strategic research arena on "Energy Efficient Computing Systems (EECS)" at the IME-Faculty.
- Project leader for the Horizon 2020 initiative within EECS. EECS is one of seven groups selected by NTNU to receive special support towards EU's research and innovation program Horizon 2020.
- Member of the international special interest group on Scenario Driven Design for Embedded Systems.
- Reviewer for several academic journals and conferences in my field of interest. Member of the program committees of the AICCSA and NorCAS conferences.
- Member of the organizing committee of FPGA-forum, an annual Norwegian FPGA seminar.
- EMECS, European Master in Embedded Computing Systems, an Erasmus Mundus Master Program sponsored by the European Union (EU). A cooperation between NTNU (departments at the IE faculty), University of Kaiserslautern, Germany, and University of Southampton, United Kingdom. I am deputy leader for the activities at NTNU.
- Teaching (parts of) TFE4101 Krets- og digitalteknikk, a first year course in electrical circuits and digital design.
- Coordinating TFE4141 Design av digitale systemer 1, a fourth year course on design of digital systems.
- Teaching TFE02 HW/SW Codesign med innvevde systemer, a fifth year course in HW/SW Codesign and embedded systems.
- Teaching FE8109 Design og utnyttelse av minnehierarkier i multimedia applikasjoner, a PhD student course in Design and Utilization of Memory Hierarchies in Multi-Media Applications.
- Supervising a number of students at master and PhD level.
- Chairman of the board of directors at Thelma Biotel; an ICT company specializing in telemetry.

Former Projects and Responsibilities

- Group leader of the Circuit and Radio Systems group at IES, NTNU (2014-2019).
- Work package leader for the Horizon 2020 Future and Emerging Technologies (FET) project READEX (Run-time Exploitation of Application Dynamism for Energy-efficient Exascale computing).
- Principal researcher for the Horizon 2020 Leadership in Enabling and Industrial Technologies (LEIT) project Tulipp (Towards Ubiquitous Low-power Image Processing Platforms).
- Member of the board of the enabling technologies strategic initiative NTNU Digital (2016-2019).
- Member of IME-SIG Embedded and IME-SIG Multipro; two cross-departmental Special Interest Groups at the IME-Faculty (2009-2016). I supervised one PhD student and was co-supervisor of another PhD student financed through IME-SIG Embedded.
- Special Session Chair at the European Conference on Circuit Theory and Design, 2015
- Member of the organizing committee of the HiPEAC Computing Systems Week in Oslo, Norway, May 2015.
- Secretary and administrator of Mikroelektronikkforum, a department – industry contact group in the field of microelectronics (2003-2015).
- Deputy board member of the corporate board at Sintef; the largest independent research organization in Scandinavia with approximately 2000 employees (2011-2015).
- Coordinating and teaching (parts of) TFE4105 Digitalteknikk og datamaskiner, a second year course in digital design (2001-2014).
- Coordinating and teaching TFE4140 Modellering og analyse av digitale kretser, a third year course on modeling and analysis of digital systems (2002-2012).
- Member and Deputy Chair of the Board for Research and Education of Researchers at the IME-Faculty (2002-2012).
- Member of the program committee of the CODES+ISSS conference (2010-2012).
- Member of the board of directors at Thelma AS between 2000 and 2011 (chairman between 2001 and 2009).
- CROPS, CRoss-layer OPtimization in Short-range wireless sensor networks, a Nordic research project with six PhD students. I was co-supervisor for one PhD student (2008-2010).
- Cuban, Co-optimized Ubiquitous Broadband Access Networks, a Norwegian Research Council project in cooperation with five other professors and associate professors at our department. Eight PhD candidates were educated within this project. I supervised two of them (2004-2007).
- Commissioner for equal opportunities at the IME-Faculty (2002-2005)
- EMBLA, a Norwegian Research Council project focusing on EMBedded systems design, modeling, Languages and Analysis (2003-2005). It had participation from ten Norwegian industrial companies in addition to educational and research establishments.
- CoDeVer, a Norwegian Research Council project focusing on Codesign and Coverification (1999-2002). It had participation from ten industrial companies in addition to educational and research establishments.
- Member of the board of directors at Eidsvoll Electronics AS (1995-1999 and 2003-2007).
- Member of the IME-Faculty Board (1999).

PhD-students

2019 – Present: Supervisor at NTNU for Stian Sørensen, a dual PhD student with TU Kaiserslautern, Germany, on a Formal approach to profiling hardware usage for efficient embedded systems design.

2013 – 2019: Co-supervisor for Nico Reissmann on Compiling with the Regionalized Value State Dependence Graph

2013 – 2018: Supervisor for Yahya Yassin on Techniques for scenario prediction and switching in system scenario based designs.

2013 – 1018: Co-supervisor for Yaman Umuroglu on Energy Efficient Heterogeneous Multi-Core Architectures.

2011 – 2016: Supervisor for Iason Filippopoulos on Exploration of energy efficient memory organizations using system scenarios.

2011 – 2016: Co-supervisor for Mladen Skelin on Temporal analysis of real-time streaming applications.

2010 – 2017: Co-supervisor for Alexandru Ciprian Iordan on Improving the Energy-efficiency of Task Based Programming Applications on Chip Multiprocessors.

2007 - 2018: Supervisor for Elena Hammari on Identification of data-variable based scenarios for design of dynamic embedded systems.

2006 – 2010: Co-supervisor for Changmian Wang on co-optimization of link adaptation and resource allocation schemes, and node circuitry power consumption.

2004 – 2009: Supervisor for Asghar Havshki on Power Consumption Issues in FIR Filters with Application to Communication Receivers: Complexity, Word length, and Switching Activity.

2004 – 2008: Supervisor for Saeeid Tahmasbi Oskuii on Design of Low-Power Reduction Trees in Parallel Multipliers

2002 - 2007: Supervisor for Qubo Hu on Hierarchical Memory Size Estimation for Loop Transformation and Data Memory Platform Exploration.

Publications

Journal Papers

- Hammari, E., Kjeldsberg, P.G., and Catthoor, F., "Run-Time Precomputation of Data-Dependent Parameters in Embedded Systems", ACM Transactions on Embedded Computing Systems (TECS), Volume 17, Issue 3, June 2018, Article No. 68.
- Yassin, Y., Catthoor, F., Kloosterman, F., Couto, J., Sun, J-J., Kjeldsberg, P.G., and Van Helleputte, N., "Technique for automatic data reduction of wireless read-out in high-density electrode arrays", ACM Transactions on Embedded Computing Systems (TECS), Volume 17, Issue 3, June 2018, Article No. 67.
- Yassin, Y., Kjeldsberg, P.G., Perkis, A., and Catthoor, F., "Techniques for dynamic hardware management of streaming media applications using a framework for system scenarios", Elsevier Microprocessors and Microsystems, Vol. 56, February 2018, pp. 157 – 168.
- Hasib A.A., Natvig, L., Kjeldsberg, P.G., and Cebrián, J.M., "Energy Efficiency Effects of Vectorization in Data Reuse Transformations for Many-Core Processors - A Case Study", Journal of Low Power Electronics and Applications, 2017, 7(1), 5, pp. 1-21.
- Schuchart, J., Gerndt, M., Kjeldsberg, P.G., Lysaght, M., Horák, D., Říha, L., Gocht, A., Sourouri, A., Kumaraswamy, M., Chowdhury, A., Jahre, M., Diethelm, K., Bouizi, O., Mian, U.S., Kruzík, J., Sojka, R., Beseda, M., Kannan, V., Bendifallah, Z., Hackenberg, D., and Nagel, W.E., "The READEX Formalism for Automatic Tuning for Energy Efficiency", Springer Computing Journal, Special issue on Energy Reduction Techniques for Exa-Scale Computing - Theory and Practice.(2017) 99:727-745.
- Filippopoulos, I., Sharma, N., Catthoor, F., Kjeldsberg, P.G., and Panda, P.R., "Integrated Exploration Methodology for Data Interleaving and Data-to-Memory Mapping on SIMD architectures", ACM Transactions on Embedded Computing Systems, 2016. Vol. 15, No. 3, 59:1-23.

- Filippopoulos, I., Catthoor, F., and Kjeldsberg, P.G., "Exploration of energy efficient memory organisations for dynamic multimedia applications using system scenarios", Design Automation for Embedded Systems, Springer, 2014, DOI: 10.1007/s10617-014-9145-6.
- Kjeldsberg, P.G., Catthoor, F., Verdoolaege, S., Palkovic, M., Vandecappelle, A., Hu, Q., and Aas, E.J., ”Guidance of Loop Ordering for Reduced Memory Usage in Signal Processing Applications”, Springer Journal of Signal Processing Systems Vol. 53, No. 3, December 2008, pp. 301 - 321.
- Balasa, F., Kjeldsberg, P.G., Palkovic, M., Vandecappelle, A., Hu, Q., Zhu, H., and Catthoor, F., “Storage Estimation and Design Space Exploration Methodologies for the Memory Management of Signal Processing Applications”, Springer Journal of Signal Processing Systems, Vol. 53, No. 1-2, pp. 51 - 71. Invited submission after ASAP 2006 conference.
- Hu, Q., Kjeldsberg, P.G., Vandecappelle, A., Palkovic, M., and Catthoor, F., "Incremental Hierarchical Memory Size Estimation for Steering of Loop Transformations", ACM Transactions on Design Automation of Electronic Systems, Vol. 12, No. 4, September 2007, pp. 50 - 50:27.
- Thörnberg, B. , Palkovic, M., Hu, Q., Olsson, L., Kjeldsberg, P.G., O’Nils, M, and Catthoor, F., "Bit-Width Constrained Memory Hierarchy Optimization for Real-Time Video Systems", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 26, No. 4, April 2007, pp. 781 – 800.
- Dybdahl, H., Kjeldsberg, P.G., Grannæs, M., and Natvig, L., "Destructive-Read in Embedded DRAM, Impact on Power Consumption", Journal of Embedded Computing, IOS Press, Vol. 2, No. 2, 2006, pp. 249 - 260.
- Thörnberg, B., Hu, Q., Palkovic, M., O’Nils, M., and Kjeldsberg, P.G., “Polyhedral space generation and memory estimation from interface and memory models of real-time video systems”, Elsevier Journal of Systems and Software, Vol. 79, No 2, February 2006, 231-245.
- Kjeldsberg, P.G., Catthoor, F., and Aas, E.J., "Storage Requirement Estimation for Optimized Design of Data Intensive Applications", ACM Transactions on Design Automation of Electronic Systems, Vol. 9, No. 2, April 2004, pp. 133-158.
- Kjeldsberg, P.G., Catthoor, F., and Aas, E.J., "Data Dependency Size Estimation for use in Memory Optimization", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 22, No. 7, July 2003, pp. 908-921.
- Panda, P.R., Catthoor, F., Dutt, N.D., Danckaert, K., Brockmeyer, E., Kulkarni, C., Vandercappelle, A., and Kjeldsberg, P.G. "Data and memory optimization techniques for embedded systems", ACM Transactions on Design Automation of Electronic Systems, Vol. 6, No 2, April 2001, pp. 149 - 206 (the most downloaded article from ACM TODAES (568 times) between July 02, 2008 and 2009).

Conference Papers

- Seyedi, A., Aunet, S., and Kjeldsberg, P.G., "Nwise: an Area Efficient and Highly Reliable Radiation Hardened Memory Cell Designed for Space Applications", accepted for publication at IEEE Nordic Circuits and Systems Conference, NorCAS 2019, Helsinki, Finland, October 2019.
- Amundsen, K.K., Myklebust, G., Kjeldsberg, P.G., and Jahre, M., "Finger Finder: A Low-Energy Peak Detection Accelerator for Capacitive Touch Controllers", Third Workshop on Computer Architecture Research with RISC-V, CARRV 2019, Phoenix, USA, June 2019.
- Sourouri, M., Raknes, E.B., Reissmann, N., Langguth, J., Hackenberg, D., Schöne, R., and Kjeldsberg, P.G., "Towards Fine-grained Dynamic Tuning of HPC Applications on Modern Multi-Core Architectures", SC17, The International Conference for High Performance Computing, Networking, Storage and Analysis, Denver, CO, USA, November 2017.
- Kjeldsberg, P.G., Gocht, A., Gerndt, M., Riha, L., Schuchart, J., and Mian, U.S., "READEX: Linking Two Ends of the Computing Continuum to Improve Energy-efficiency in Dynamic Applications", 2017 Design Automation and Test in Europe, DATE 2017, Lausanne, Switzerland, March 2017.

- Yassin, Y., Kjeldsberg, P.G., Perkis, A., Catthoor, F., “Dynamic hardware management of the H264/AVC encoder control structure using a framework for system scenarios”, accepted for publication at the Euromicro Conference on Digital System Design, DSD 2016, Limassol, Cyprus, August-September 2016.
- Oleynik, Y., Gerndt, M., Schuchart, J., Kjeldsberg, P.G., and Nagel, W., "Run-time Exploitation of Application Dynamism for Energy-efficient Exascale Computing (READEX)", IEEE 18th International Conference on Computational Science and Engineering, CSE 2015, Porto, Portugal, October 2015.
- Yassin, Y., Kjeldsberg, P.G., Catthoor, F., “System Scenario Framework evaluation on EFM32 using the H264/AVC encoder control structure”, The 22nd European conference on circuit theory and design, ECCTD2015, Trondheim, Norway, August 2015.
- Zompakis, N., Filippopoulos, I., Kjeldsberg. P.G., Catthoor, F., and Soudris, D., "Systematic Exploration of Power-Aware Scenarios for IEEE 802.11ac WLAN Systems", The 17th EUROMICRO Conference on Digital System Design (DSD), Verona, Italy, August 2014.
- Filippopoulos, I., Catthoor, F., and Kjeldsberg. P.G., "Exploration of energy efficient memory organisations for dynamic multimedia applications using system scenarios", Memory Architecture and Organization Workshop, MEAOW2013, Embedded Systems Week, Montreal, Canada, October 2013.
- Filippopoulos, I., Catthoor, F., Kjeldsberg. P.G., Hammari, E., and Huisken, J., "Memory-Aware System Scenario Approach Energy Impact", IEEE NORCHIP Conference, NORCHIP 2012, Copenhagen, Denmark, November 2012.
- Hasib A.A., Kjeldsberg, P.G., and Natvig, L., "Performance and Power Efficiency Analysis of Data Reuse Transformation Methodology on Multicore Processor", 1st Workshop on On-chip Memory Hierarchies and Interconnects: organization, management and implementation, OMHI 2012, at Euro-Par 2012, Rhodes, Greece, August 2012. Published in Springer Lecture Notes in Computer Science, Vol. 7640, 2013, pp. 337 - 346.
- Hammari, E., Catthoor, F., Kjeldsberg, P.G., Huisken, J., Tsakalis, K., and Iasemidis, L., "Identifying Data-Dependent System Scenarios in a Dynamic Embedded System", The International Conference on Engineering of Reconfigurable Systems and Algorithms, ERSA'12, Las Vegas,USA, July 2012.
- Hammari, E., Catthoor, F., Iasemidis, L., Kjeldsberg, P.G., Huisken, J., and, Tsakalis, K., "Realization of dynamical electronic systems", presented at The 1st International Conference on New Frontiers in Physics, Kolymbari, Crete, Greece, June 2012. Published in the European Physical Journal (EPJ) Web of Conferences, No 70, Apr. 2014, pp. 1-10.
- Hammari, E., Catthoor, F., Huisken, J., and Kjeldsberg. P.G., "Application of Medium-Grain Multiprocessor Mapping Methodology to Epileptic Seizure Predictor", IEEE NORCHIP Conference, NORCHIP 2010, Tampere, Finland, November 2010, 6 pages.
- Yassin, Y.H., Kjeldsberg, P.G., Hulzink, J., Romero, I., and Huisken, J., "Ultra Low Power Application Specific Instruction-Set Processor Design for a Cardiac Beat Detector Algorithm", IEEE NORCHIP Conference, NORCHIP 2009, Trondheim, Norway, November 2009, 4 pages.
- Miniskar, N.R., Hammari, E., Munaga, S., Mamagkakis, S., Kjeldsberg, P.G., and Catthoor, F., "Scenario Based Mapping of Dynamic Applications on MPSoC: A 3D Graphics Case Study", 9th International Workshop on Embedded Computer Systems: Architectures, Modeling, and Simulation, SAMOS 2009, July 2009, Samos, Greece. Published in Springer Lecture Notes in Computer Science, Vol. 5657, 2009, pp. 48 - 57.
- Havashki, A., Lundheim, L., Kjeldsberg, P.G., Gustafsson, O., and Øien, G.E., "Analysis of switching activity in DSP signals in the presence of noise", IEEE Region 8 EUROCON 2009 Conference, St. Petersburg, Russia, May 2009, pp. 253 - 258.
- Havashki, A., Lundheim, L., Kjeldsberg, P.G., and Øien, G.E., "Effects of Finite Coefficient Word Length on Channel Estimator Performance", IEEE International Conference on Signal Processing, ICSP2008, Beijing, China, October 2008, pp. 402 - 405.
- Oskuii, S.T., Kjeldsberg, P.G., Lundheim, L., and Havashki, A., "Power Optimization of Parallel Multipliers in Systems with Variable Word-length", International Workshop on Power And

Timing Modeling, Optimization and Simulation, PATMOS 2008, Lisbon, Portugal, September 2008. Published in Springer Lecture Notes in Computer Science, Vol. 5349, January 2009, pp. 103 - 115.

- Oskuii, S.T., Johansson, K., Gustafsson, O., and Kjeldsberg, P.G., "Power Optimization of Weighted Bit-Product Summation Tree for Elementary Function Generator", IEEE International Symposium on Circuits and Systems, ISCAS 2008, Seattle, USA, May 2008, pp. 1240 - 1243.
- Oskuii, S.T., Kjeldsberg, P.G., and Gustafsson, O., "Power Optimized Partial Product Reduction Interconnect Ordering in Parallel Multipliers", IEEE NORCHIP Conference, NORCHIP 2007, Aalborg, Denmark, November 2007, 6 pages.
- Havashki, A., Kjeldsberg, P.G., Øien, G.E., Lundheim, L., and Nymoen, J.T., "On the impact of fixed point DSP implementation on required channel estimator complexity in communication receivers", IEEE International Symposium on Wireless Communication Systems, ISWCS 2007, Trondheim, Norway, October 2007, pp. 469 - 474.
- Gustafsson, O., Oskuii, S.T., Johansson, K., and Kjeldsberg, P.G., "Low-Power Realization of FIR Filters with Correlated Input Data on MAC-Based Architectures", International Workshop on Power And Timing Modeling, Optimization and Simulation, PATMOS 2007, Gothenburg , Sweden, September 2007. Printed in Lecture Notes in Computer Science, Vol 4644/2007, pp. 526-535, Springer.
- Hu, Q., Vandecappelle, A., Kjeldsberg, P.G., Catthoor, F., and Palkovic, M., "Fast Memory Footprint Estimation based on Dependency Distance Vector Calculation", Design, Automation and Test in Europe, DATE 2007, Nice, France, April 2007, pp. 379-384.
- Oskuii, S.T., Kjeldsberg, P.G., and Gustafsson, O., "Transition-activity Aware Design of Reduction-stages for Parallel Multipliers", ACM Great Lake Symposium on VLSI, GLSVLSI 2007, Stresa - Lago Maggiore, Italy, March 2007, pp. 120-125.
- Oskuii, S.T., Kjeldsberg, P.G., and Aas, E.J., "Probabilistic Gate-level Power Estimation using a Novel Waveform Set Method", ACM Great Lake Symposium on VLSI, GLSVLSI 2007, Stresa - Lago Maggiore, Italy, March 2007, pp. 37-42.
- Balasa, F., Kjeldsberg, P.G., Palkovic, M., Vandecappelle, A., and Catthoor, F., "Loop Transformation Methodologies for Array-Oriented Memory Management", invited paper at IEEE 17th International Conference on Application-specific Systems, Architectures and Processors, ASAP 2006, Steamboat Springs, Colorado, USA, September 2006.
- Hu, Q., Vandecappelle, A., Palkovic, M., Kjeldsberg, P.G., Brockmeyer, E., and Catthoor, F., "Hierarchical Memory Size Estimation for Loop Fusion and Loop Shifting of Data Dominated Applications", 11th Asia and South Pacific Design Automation Conference, ASP-DAC 2006, Yokohama City, Japan, January 2006, pp. 606-611.
- Hu, Q., Brockmeyer, E., Palkovic, M., Kjeldsberg, P.G., and Catthoor, F., "Memory Hierarchy Usage Estimation for Global Loop Transformations", IEEE NORCHIP Conference, NORCHIP 2004, Oslo, Norway, November 2004, pp. 301-304.
- Hu, Q., Palkovic, M., Kjeldsberg, P.G., "Memory Requirement Optimization with Loop Fusion and Loop Shifting", 30th Euromicro conference, Rennes, France, Aug 31 - Sep 3 2004, pp. 272-278.
- Rydland, P., Palkovic, M., Kjeldsberg, P.G., Brockmeyer, E., and Catthoor, F., "Inter in-place storage size requirement estimation", IEEE NORCHIP Conference, NORCHIP 2003, Riga, Latvia, November 2003, pp. 240-243.
- Kjeldsberg, P.G., Catthoor, F., Aas, E.J., and Palkovic, M. "STOREQ: STOrage REQuirement Estimation and Optimization Tool for Data Intensive Applications", Design, Automation and Test in Europe, DATE 2002, Paris, France, March 2002, Designers' Forum, pp. 256.
- Kjeldsberg, P.G., Catthoor, F., and Aas, E.J. "Detection of Partially Simultaneously Alive Signals in Storage Requirement Estimation for Data Intensive Applications", 38th Design Automation Conference, DAC 2001, Las Vegas, NV, USA, June 2001, pp. 365-370.
- Kjeldsberg, P.G., Catthoor, F., and Aas, E.J. "Automated Data Dependency Size Estimation with a Partially Fixed Execution Ordering", International Conference on Computer Aided Design, ICCAD 2000, San Jose, USA, November 2000, pp. 44-50.

- Kjeldsberg, P.G., Catthoor, F., and Aas, E.J. "Application of High-Level Memory Size Estimation for Guidance of Loop Transformations in Multimedia Design", IEEE Nordic Signal Processing Symposium, NORSIG 2000, Kolmården, Sweden, June 2000, pp. 371-374.
- Kjeldsberg, P.G., Catthoor, F., and Aas, E.J. "Storage Requirement Estimation for Data Intensive Applications with Partially Fixed Execution Ordering", International Workshop on HW/SW Codesign, CODES 2000, San Diego, USA, May 2000, pp. 56-60.

Books and Book Chapters

- Catthoor, F., Basten, T., Zompakis, N., Geilen, M., and Kjeldsberg, P.G., "System-Scenario-based Design Principles and Applications", Springer Nature Switzerland AG, 2019, 230 pages, ISBN 978-3-030-20342-9. Co-author of chapters 1, 3, 4 and 6.
- Mjølsnes, S.F., “A Multidisciplinary Introduction to Information Security", CRC Press, New York, USA, 2011, ISBN 978-1-4200-8590-7. Chapter 2: Aas, E.J. and Kjeldsberg, P.G., "Security Electronics", pp. 19-35.
- Catthoor, F., Danckaert, K., Kulkarni, C., Brockmeyer, E., Kjeldsberg, P.G., Van Achteren, T., and Omnes, T., "Data Access and Storage Management for Embedded Programmable Processors", Kluwer Academic Publishers, Dordrecht, The Netherlands, 2002, ISBN 0-7923-7689-7.
- Kjeldsberg, P.G., "Storage Requirement Estimation and Optimization for Data Intensive Application", Doctoral Thesis, Norwegian University of Science and Technology, Defended March 23, 2001, ISBN 82-7984-174-1.

Miscellaneous

- Kjeldsberg, P.G., "Mikroelektronikkprisen 2018, Pris for effektiv DMA-kjerne", Elektronikk, nr. 3, 2019, pp. 16-17 ("Microelectronics Prize 2019", published in the Norwegian magazine Elektronikk, No. 3, 2019).
- Kjeldsberg, P.G., “READEX gjør dynamiske HPC-applikasjoner energieffektive", Elektronikk, nr. 10, 2018, pp. 30-31 (“READEX makes dynamic HPC applications energy efficient”, published in the Norwegian magazine Elektronikk, No. 10, 2018).
- Kjeldsberg, P.G., "Mikroelektronikkprisen 2017", Elektronikk, nr. 4, 2018, pp. 12 ("Microelectronics Prize 2017", published in the Norwegian magazine Elektronikk, No. 4, 2018).
- Kjeldsberg, P.G., “Mikroelektronikkprisen 2016", Elektronikk, nr. 4, 2017, pp. 14 ("Microelectronics Prize 2016", published in the Norwegian magazine Elektronikk, No. 4, 2017).
- Kjeldsberg, P.G., "Mikroelektronikkprisen 2015", Elektronikk, nr. 4, 2016, pp. 16 ("Microelectronics Prize 2015", published in the Norwegian magazine Elektronikk, No. 4, 2016).
- US Patent 9,244,701 B2: Catthoor, F., Bebelis, E., Van Thillo, W., Raghavan, P., Fasthuber, R., Hammari, E., Kjeldsberg, P.G., and Huisken, J., "Method for System Scenario Based Design of Dynamic Embedded Systems".
- Kjeldsberg, P.G., "Mikroelektronikkprisen 2014", Elektronikk, nr. 3, 2015, pp. 14 ("Microelectronics Prize 2014", published in the Norwegian magazine Elektronikk, No. 3, 2015).
- Kjeldsberg, P.G., "EU-forskning og innovasjon mot nye horizonter", Elektronikk, nr. 5, 2014, pp. 36-37 ("EU research and innovation towards new horizons", published in the Norwegian magazine Elektronikk, No.5, 2014).
- Kjeldsberg, P.G., "Mikroelektronikkprisen 2013", Elektronikk, nr. 3, 2014, pp. 16 ("Microelectronics Prize 2013", published in the Norwegian magazine Elektronikk, No. 3, 2014).
- Patent pending in Europe: Catthoor, F., Bebelis, E., Van Thillo, W., Raghavan, P., Fasthuber, R., Hammari, E., Kjeldsberg, P.G., and Huisken, J., "Method for System Scenario Based Design of Dynamic Embedded Systems". Application numbers EP 12176304.
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- Kjeldsberg, P.G., "Mikroelektronikkprisen 2006", Elektronikk, nr. 11, 2006, pp. 18 ("Microelectronics Prize 2006", published in the Norwegian magazine Elektronikk, No. 11, 2006).
- Kjeldsberg, P.G., "STOREQ: STOrage REQuirement Estimation and Optimization tool for Data Intensive Applications", European Research Consortium for Informatics and Mathematics, ERCIM News, No. 52, January 200, pp. 29-30.
- Kjeldsberg, P.G., "DATE i fortsatt vekst", Elektronikk, nr. 4, 2002, 18-20 ("DATE in continued growth", published in the Norwegian magazine Elektronikk, No. 4, 2002).
- Kjeldsberg, P.G., "En introduksjon til codesign: hva, hvordan og hvorfor?", Elektronikk, nr. 12, 1998, 48-54 ("An Introduction to Codesign: What, How, and Why?", published in the Norwegian magazine Elektronikk, No. 12, 1998).

Presentations, Training Courses, Research Visits, and PhD Evaluation Committees

July 2019 – June 2020: Visiting professorial fellow at School of Computer Science and Engineering, University of New South Wales, Sydney, Australia. Hosted by Professor Sri Parameswaran.

November 2018: Committee member and administrator of PhD evaluation committee for Bahram Najafiuchevler at NTNU.

March 2017: Design Automation and Test in Europe, DATE 2017, Lausanne, Switzerland. I gave a presentation on “READEX: Linking Two Ends of the Computing Continuum to Improve Energy-efficiency in Dynamic Applications".

September 2016: Member of PhD evaluation committee for Andréas Karlsson at Linköping University, Sweden.

January 2016: Dagstuhl Seminar, Dark Silicon: From Embedded to HPC Systems, Schloss Dagstuhl – Leibniz-Zentrum für Informatik, Wadern, Germany. I gave a presentation on “Scenarios Based Design of Dynamic Embedded Systems”.

May 2015: Committee member and administrator of PhD evaluation committee for Milica Orlandić at NTNU.

February 2015 FPGA-forum (Norwegian FPGA seminar). I gave a presentation regarding design and integration of accelerators on the SHMAC multiprocessor platform. I was also chair in one of the sessions.

October 2013: HiPEAC Computing Systems Week in Tallin, Estland. I gave a presentation on “Scenario based design and evaluation of dynamic applications on heterogeneous multi-processor systems”.

June 2013: Member of PhD evaluation committee for Khursheed Khurseed at Mid Sweden University, Sundsvall, Sweden.

January 2013:	Member of PhD evaluation committee for Tung Thanh Hoang at Chalmers University, Gothenburg, Sweden.
September 2012:	Opponent at the PhD defense of Thomas Canhao Xu at University of Turku, Finland.
August 2012-March 2013:	Visiting researcher at imec Netherlands, Holst Centre, High Tech Campus, Eindhoven. Hosted by Senior Researcher Jos Hulzink.
May 2012:	Administrator of PhD evaluation committee for Alfonso Martinez del Hoyo Canterla at NTNU.
February 2011	FPGA-forum (Norwegian FPGA seminar). I gave a presentation regarding use of Altera's DE2-board for embedded demonstrators. I was also chair in one of the sessions.
November 2010	Third Swedish Workshop on Multi-Core Computing – MCC'10. I participated in a panel discussing "Embedded computing: caching mechanisms vs. local stores, or something new?".
September 2010	Meeting between the Norwegian Research Council and the Rector (Dean) at NTNU. I gave a presentation of how fundamental research and education in the field of microelectronics is put to use in industry.
February 2010:	FPGA-forum (Norwegian FPGA seminar). I gave a presentation explaining how we use FPGAs in the education at our department. I was also chair in one of the sessions.
November 2009:	IEEE NORCHIP Conference, Trondheim, Norway. I was member of the program committee and chair in two sessions.
October 2008:	FPGA-forum (Norwegian FPGA seminar). I was chair in one of the sessions.
June 2007:	Administrator of PhD evaluation committee for Greg Harald Håkonsen at NTNU.
December 2006:	Administrator and member of PhD evaluation committee for Øystein Gjermundnes at NTNU.
October 2005-June 2006:	Visiting researcher at Center of Embedded Computer Systems, University of California, Irvine. Hosted by Prof. Nikil Dutt.
August 2003:	Swedish National Summer School on Multiprocessor Systems on Chip, Örebro, Sweden. I was invited to present a talk on "Optimized Design and Use of Memory Hierarchies in Data Intensive Multi-Media Applications".
October 2002:	DAK Forum (Norwegian CAD Seminar), Vidar A. Pettersen and I gave a presentation of tools and platforms for HW/SW Codesign.
March 2002:	Design Automation and Test in Europe, DATE 2002, Paris, France, March 2002. I presented the cad tool I developed during my Ph.D. at the University Booth.
June 2001:	38th Design Automation Conference, DAC 2001, Las Vegas, NV, USA. I presented a paper on "Detection of Partially Simultaneously Alive Signals in Storage Requirement Estimation for Data Intensive Applications". I also presented my work in the Ph.D. Forum and at the University Booth at the conference.
October-December 2000:	Repeated visit to IMEC in Leuven, Belgium. I continue my work with Francky Catthoor and his colleagues within the field of Data Transfer and Storage Exploration.
November 2000:	International Conference on Computer Aided Design, ICCAD 2000, San Jose, USA. I presented a paper on Automated Data Dependency Size Estimation with a Partially Fixed Execution Ordering

June 2000:	IEEE Nordic Signal Processing Symposium, NORSIG 2000, Kolmården, Sweden. I presented a paper on “Application of High-Level Memory Size Estimation for Guidance of Loop Transformations in Multimedia Design”.
May 2000:	The 8th International Workshop on HW/SW Codesign, CODES 2000, San Diego, USA. I presented a paper on “Storage Requirement Estimation for Data Intensive Applications with Partially Fixed Execution Ordering”.
October 1999:	DAK Forum (Norwegian CAD Seminar), I gave a presentation of the "Data Transfer and Storage Exploration" from IMEC.
September 1999:	How to write high-performance low-power multimedia application code, IMEC, Belgium
January-July 1999:	Visiting IMEC in Leuven, Belgium. I worked with Francky Catthoor and his colleagues within the field of Data Transfer and Storage Exploration
January 1999:	C++ based Hardware Design of Complex Digital Systems, IMEC, Belgium
October 1998:	DAK Forum (Norwegian CAD Seminar), I gave a presentation of codesign methodologies, emphasizing topics that are presently important in the research community.
August 1998:	NATO Advanced Study Institute course in System Level Synthesis, Il Ciocco, Italy.
June 1998:	ARM Microprocessor Training Seminar, Stansted, England
October 1996:	Hardware/Software Codesign Advanced Course, Grenoble, France
October 1995:	DAK Forum (Norwegian CAD Seminar), I presented Eidsvoll Electronics' experience going from UNIX to Windows NT as CAD OS.

My Background and Research Interests

After finishing high school, I served one and a half year in the Norwegian army. One year is obligatory in Norway, but wanting to get something useful out of my time there, I decided to be trained as a sergeant. Having finished my one-year, I continued to serve as a sergeant until the university semester started in the fall. Already in this first semester of my master study I realized that digital design was my main interest. In the following years I specialized in microelectronics and digital design methodologies in particular. For my master thesis I made a fast compiler-based functional simulator for sequential circuits. The topic was proposed by the design company Nordic Semiconductor ASA. During summer employment at Telenor Research and Development, the national telecommunications operator's research center, I also gained more experience with design and design tools.

When I left the university in the spring of 1992 I went to work with Eidsvoll Electronics AS (EIDEL) as a design engineer. The work varied from computer aided circuit design, laboratory prototype testing, and system installation, to discussions with customers about future products and contracts. I also had responsibilities at external training courses, teaching customers how to use our equipment. The main product of my department at EIDEL was radio remote control equipment. It was typically realized as an embedded system, with a microprocessor running software and controlling analog circuits and digital logic in Programmable Logic Devices.

In august 1996 I started working towards my doctoral degree under supervision of Professor Einar J. Aas in the Circuit and Systems group of Department of Physical Electronics, NTNU. Since I left the university four years earlier, I had planned to continue my studies after having gained some industrial experience. My work as a sergeant, as an amateur actor during my student days, and as a lecturer at EIDEL, had also given me practice and interest in public speaking and teaching. Being important parts of the duties at a university, this also encouraged me to return. I was hired on an open department grant, and consequently had quite a bit of influence on what my research topic

should be. While I worked at EIDEL, I had met with the challenges of embedded systems design, experiencing the lack of tools and methodologies when designing systems encompassing both hardware and software. This was the main reason why Hardware/Software Codesign was selected as my field of research.

Most of my first two years was spent taking obligatory doctoral courses, working for the department, and getting a good understanding of my subject. I was then able to start more in-depth research. My group at the university has wide experience working with low power issues, in particular for Digital Signal Processing applications. Research on circuit partitioning has also been a main concern. This local knowledge facilitated my own research in power estimation for hardware/software partitioning. In January 1999 I went for a six month research stay at IMEC in Leuven, Belgium. Here I worked with Francky Catthoor (IEEE Fellow and Adjunct Professor at KU Leuven) and his System Exploration for Memory and Power (SEMP) group. Their research focus was design methodologies for embedded multimedia systems. For this class of applications, data transfer and storage is a dominating cost factor. This is the case for *chip size*, since large memories are usually needed, *performance*, since accessing the memories may very well be the main bottleneck, and *power consumption*, since the memories and buses consume large quantities of power. A Data Transfer and Storage Exploration (DTSE) methodology was being developed for high level system design. The application is described in C code, which is then step by step transformed into a more storage optimal implementation. During the stay I changed the focus of my research somewhat to be able to work closer with the people in the SEMP group. At each optimization step in the DTSE methodology, estimation of memory size is needed to guide the selection of the best solution. My work was thus concerned with storage requirement estimation: *How may we achieve a fast but accurate estimate of the storage requirements, given a high level C description as input?* A number of conference and journal papers were published presenting the results. I also developed a prototype CAD tool demonstrating the feasibility of the developed techniques. Based on this work I wrote and defended my Doctoral Thesis. It was also included as a chapter in a book published by Kluwer Academic Publishers describing the current status of the DTSE methodology. Parts of the DTSE methodology has since then been commercialized through the companies PowerEscape and CoWare.

After finishing my PhD, I was permanently employed as an Associate Professor at Department of Physical Electronics, NTNU (now part of Department of Electronic Systems). The first PhD-student I supervised, Qubo Hu, continued the cooperation with IMEC within the field of memory size estimation and optimization. Before successfully defending his thesis in April 2007, Hu had several prolonged stays at IMEC and also published several conference and journal papers. In the memory optimization research area Qubo Hu and I also cooperated with Department of Information Technology and Media at Mid-Sweden University, Sweden. The cooperation with IMEC continued through the work of PhD-student Elena Hammari. With her the direction changed somewhat as she focuses on utilization of computational resources in heterogeneous multi-processor system on chip. She exploits and extends a methodology for system scenario based design that has for some years been developed by imec and partners within the Special Interest Group on Scenario Driven Design for Embedded Systems. Through detailed profiling and analysis of dynamic behavior of applications and platforms at design time, a set of system scenarios are defined that includes optimized configuration of platform parameters as well as techniques for detecting upcoming scenarios and switching between scenarios. At run-time the upcoming scenario is detected, and the system configured accordingly for energy efficient exploitation.

Hammari defended her thesis in 2018. In addition to having me as supervisor and Francky Catthoor as co-supervisor from IMEC, Hammari had Professor Lasse Natvig from Department of Information Technology and Computer Science (IDI), NTNU, as co-supervisor. Furthermore, her work is supported by the group working in the field of real-time systems at Department of Engineering Cybernetics, NTNU. This demonstrates the multi-disciplinary quality of the project, and its importance in various fields. The project also fitted naturally into the fields of interest of two Special Interest Groups at the IME-faulty, IME-SIG Embedded and IME-SIG Multipro. Within the scope of these groups I am also co-supervisor of PhD-student Alexandru Iordan who has Lasse

Natvig as his main supervisor. In August 2011 two new PhD-students started working with projects financed through IME-SIG Embedded and in cooperation with IMEC. I have been the main supervisor of Iason Filippopoulos focusing on utilization of heterogeneous multi-processor system on chip platforms for dynamic embedded applications, and the co-supervisor of Mladen Skelin working on worst-case performance analysis of scenario-aware real-time streaming applications. Skelin has Sverre Hendseth at Department of Engineering Cybernetics as his main supervisor. Both had Francky Catthoor as co-supervisor from IMEC and continued the work on system scenario based design in a similar way as Hammari. They were also both enrolled in a dual-PhD program according to a cotutelle agreement between NTNU and KU Leuven. After defending their theses in 2016 they hence received PhD degrees from both universities.

In February 2011 I was accepted as a member of the HiPEAC (High-Performance and Embedded Architecture and Compilation) European Network of Excellence. This is an EU Seventh Framework Program network, which gathers leading European academic and industrial groups to collaborate on joint research projects, and to shape the future of computing systems in Europe.

The IME-faculty at NTNU announced a call for proposals to strategic research areas in 2012. The plan was to select a limited number of particularly relevant “lighthouse projects” that would be given special support to further enhance their research potential. Together with, among others, Lasse Natvig and Magnus Jahre at the Computer Architecture and Design (CARD) group at IDI, I participated in a proposal on Energy Efficient Computing Systems (EECS). We were selected as strategic research area. In EECS we put much effort into developing a Single-ISA Heterogeneous Many-core Computer (SHMAC) as a platform for diverse research activities. Within the scope of EECS I was supervisor for PhD-student Yahya Yassin and co-supervisor for PhD-students Yaman Umuroglu and Nico Reissmann. Yassin continued the cooperation on system scenario based design with IMEC in Belgium, was enrolled in the dual PhD program, and had Francky Catthoor as co-supervisor. Magnus Jahre was also co-supervisor for Yassin as well as main supervisor for Umuroglu and Reissmann. Yassin and Umuroglu defended their theses in 2018, while Reissmann had his defense in 2019.

As will be described later on, there has been a long term cooperation between Department of Electrical and Computer Engineering at Technische Universität Kaiserslautern (TUK) in Germany and our department at NTNU, manly through master education. In 2019 this was extended with a cotutelle agreement for a dual PhD program between the two universities. At the same time, Stian Sørensen was enrolled as the first student working on a formal approach to profiling hardware usage for efficient embedded systems design. He has TUK as his home university with Professor Wolfgang Kunz as supervisor. I am supervisor at NTNU, where he will be hosted between November 2020 and April 2022.

In 2013 EECS was selected as one of seven groups at NTNU to be given special support in our effort to write successful applications to EU’s research and innovation program Horizon 2020. Both Magnus Jahre and I are currently relived from most of our teaching duties to be able to focus on Horizon 2020 applications. I am project leader for this activity within EECS. As part of this EECS effort a process was started in the winter of 2014 to find partners for a project that could apply the system scenario methodologies developed for embedded systems in the High Performance Computing (HPC) domain. We quickly came in contact with Joseph Schuchart from Professor Wolfgang Nagel’s Center for Information Services and High Performance Computing at Technische Universität Dresden in Germany who were preparing a project with certain similarities. We decided to work together, and with partners from Technische Universität München, Germany, Technicka Univerzita Ostrava, Czech Republic, National University of Irland, Galway, Intel Corporation SAS, France, and Gesellschaft für numerische Simulation mbH, Germany, we submitted a research and innovation action proposal to the Future and Emerging Technologies (FET) call on HPC Core Technologies, Programming Environments and Algorithms for Extreme Parallelism and Extreme Data Applications (FETHPC 1 – 2014). We received excellent feedback from the reviewers and a score of 14 out of 15 possible points. The project Runtime Exploitation of Application Dynamism for Energy-efficient eXascale computing (READEX) was selected for

funding, running from September 2015 to August 2018. I led a work package on run-time detection and switching. At NTNU Mohammed Sourouri worked as a post.doc on READEX, while Nico Reissmann worked as researcher. The project resulted in advanced methodology and tool development enabling substantial reductions in HPC energy consumption, as well as active publication at conferences and in journals.

The EECS group has also succeeded in having a second Horizon 2020 project accepted. Magnus Jahre at IDI is work package leader in the project Towards Ubiquitous Low-power Image Processing Platforms (Tulipp). I participate as principal researcher. Tulipp is a Leadership in Enabling and Industrial Technologies (LEIT) innovation project coordinated by Thales in France, and with partners from Synective Labs, Sweden, Ruhr University Bochum, Germany, Efficient Innovation, France, Sundance Multiprocessor Technology Ltd, England, HIPPEROS SA, Belgium, Fraunhofer Gesellschaft, Germany, and NTNU. Tulipp run between February 2016 and January 2019. At NTNU Asbjørn Djupdal and Ananya Muddukrishna worked as post.doc researchers, developing a design optimization tool-suite for the image processing platform, including equipment for energy profiling and analysis.

A somewhat different line of work that has always been an important research interest for me is optimized implementation of digital signal processing applications. In 2003 I participated in writing the proposal for the CUBAN project (Co-optimized Ubiquitous Broadband Access Networks) together with the signal processing group at our department. The CUBAN initiative suggested the establishment of a ubiquitous wireless broadband access network based upon existing infrastructure. One major activity in this project focused on short range wireless links where processing power in the terminals is comparable to radiated power plus power dissipated in the transmitter. This situation calls for co-optimization over several disparate fields, such as modulation, coding, circuit design, and memory management. I was involved in the hardware/software implementation and optimization part of the project, and supervised PhD-students Saeeid Tahmasbi Oskuii and Asghar Havashki within this field. Parts of the work of both of them were performed in co-operation with the Electronics Systems division at Department of Electrical Engineering, University of Linköping, Sweden. Later I have also been involved in the CROPS project (CRoss-layer OPtimization in Short-range wireless sensor networks). Here I was co-supervisor for PhD-student Changmian Wang who worked with co-optimization of link adaptation and resource allocation schemes, as well as node circuitry power consumption.

In addition to the activities described above, I have participated in several internal and external projects in order to exploit our local research environment. A majority of the master students I supervise have projects that are defined and co-supervised by industrial companies. This gives rise to a collaboration rewarding for both student and company. It also assists me in staying updated on topics seen as relevant by the industry, for use in both my teaching and research.

Between October 2005 and June 2006, I was a visiting researcher at Center for Embedded Computer Systems (CECS), University of California, Irvine. I was hosted by Professor Nikil Dutt and participated in their memory and telecom related research. In August 2012 I started an eight months stay at IMEC in Eindhoven, The Netherlands, where I was hosted by Senior Researcher Jos Hulzink. My work was related to an energy efficient implementation of an epileptic seizure detection algorithm, developed by Professor Leon Iasemidis and his group at Arizona State University, USA (Iasemidis has now moved to Louisiana Tech University). From July 2019 until June 2020 I am on a 12 month stay as Visiting Professorial Fellow at School of Computer Science and Engineering, University of New South Wales, Sydney, Australia, hosted by Professor Sri Parameswaran. His group performs work in several fields in the embedded systems domain, and I am cooperating on research related to cost efficient genomic processing and approximate computing.

In parallel with my research and supervision of PhD and Master Students, much of my time is devoted to giving lectures and coordinating activities in a number of courses. From 2001 I was responsible for a second year course in digital design and computer fundemantals. When I began,

it had more than 600 students. With five big laboratory assignments for each student, comprehensive theory assignments, 20 student assistants, and four hours of lectures a week, this was a challenging task. I find this part of my work both interesting and rewarding and students in general give positive feedback regarding my teaching abilities. The 600 student course was later split, so that it had a more manageable number of students (150-200). In 2014 the course was reorganized again. I am now teaching introduction to digital design to 200 students as part of a first year course. In addition to this, I teach (parts of) a fourth year course in digital systems design (introduction to VHDL, verification strategies, and logic synthesis), a fifth year course in HW/SW codesign, and a PhD course in memory optimization techniques. I am also involved in an Erasmus Mundus European Master Embedded Computing Systems program. This program has been sponsored by the European Union (EU) and is organized as a cooperation between NTNU (departments at the IE faculty), University of Kaiserslautern, Germany, and University of Southampton, United Kingdom. I am deputy leader for the activities at NTNU.

As part of my job I also have a number of administrative duties. Between 2014 and 2019 I was leader of Circuit and Radio Systems group at our department with about 15 permanent academic staff and a similar number of PhD students and post.docs. For four years I have also been the department's member of the board of the NTNU's enabling technologies strategic initiative NTNU Digital. A main task for almost ten years was to be my department's member in the Board for research and researcher education at our Faculty. This board discusses research strategies at the Faculty level, handles PhD-student applications and progress, and in general functions as an advisory board for the Dean in research matters. This duty took quite some time but gave good insight into research strategies as well as research politics. From 2009 until I left for a research stay abroad in 2012 I was Deputy Chair for this board. As secretary of Mikroelektronikkforum, a contact forum with participation from our department and nine microelectronics companies, I led its work with improved education quality and candidate production in this field as the goal. Outside the university I am (and have been) member of the board of directors of several companies. Currently I am chairman of the board of directors of Thelma Biotel AS, a successful SME mainly working in the field of instrumentation for measurement and collection of data from fish, both in the wild and in aquaculture. For two periods (1995-1999 and 2003-2007) I was member of the board of directors of my former employer, Eidsvoll Electronic AS. I was also member of the board of directors at Thelma AS between 2000 and 2010 (chairman between 2001 and 2009) and Sense Offshore AS (between 2012 and 2015). Between 2011 and 2015 I was deputy board member of the corporate board at Sintef; the largest independent research organization in Scandinavia with approximately 2000 employees. These tasks give me experience in the challenges the industry faces, as well as in board work.

In September 2007 I applied for promotion to Professor based on acquired competence. A national committee, with assistance from two international experts, concluded that I fulfilled the requirements, and I became Professor in the field of "design and analysis of embedded hw/sw systems" in February 2009.