Curriculum vitae

1 Personal Information

Name:	Magnus Jahre
Date of birth:	03.11.1981
Nationality:	Norwegian
Web:	http://www.ntnu.edu/employees/jahre

2 Education

2010	PhD in Computer Architecture: *"Managing Shared Resources in Chip Multiprocessor Memory Systems"*, NTNU
2007	Master of Technology, Computer Science, NTNU

3 Work Experience

2010 – present	Associate Professor, Dept. of Computer and Information Science, NTNU
2010 – 2010	University Lecturer, Dept. of Computer and Information Science, NTNU
2005 – 2010	PhD Student (Integrated PhD Program), Dept. of Computer and Information Science, NTNU

4 Fellowships and Awards

2021	Accepted as member of the HiPEAC European Network of Excellence
2020	Senior Member of ACM
2020	HiPEAC paper award for *"HSM: A Hybrid Slowdown Model for Multitasking GPUs"*, ASPLOS'20
2019	Selected for NTNU's Outstanding Academic Fellows Program
2019	Awarded a "Young Research Talents" project by the Research Council of Norway
2018	HiPEAC technology transfer award for *"Non-Intrusive Power Monitoring for Embedded Systems"*
2018	HiPEAC paper award for *"Get Out of the Valley: Power-Efficient Address Mapping for GPUs"*, ISCA'18
2018	HiPEAC paper award for *"GDP: Using Dataflow Properties to Accurately Estimate Interference-Free Performance at Runtime",* HPCA'18
2018	Senior Member of the IEEE
2016	Learning Prize at the Department of Computer and Information Science for TDT4295 Computer Design Project (with Yaman Umuroglu)
2016	Outstanding Paper Award at HPCS 2016
2010	Nominated for the Exxon Mobil award for best PhD thesis at NTNU (with Marius Grannæs)
2010	Nominated for Best Paper at HiPEAC 2010
2009	4th place in the JILP Data Prefetching Championship

5 Mobility

2017-2018	Visiting researcher at Ghent University and Nordic Semiconductor
2010	Visiting researcher at the University of Tromsø

6 Institutional Responsibilities

2018 – present	Deputy head of the Computing Research Group, Dept. of Computer and Information Science, NTNU
2016 – 2017	Head of the Computing Research Group, Dept. of Computer and Information Science, NTNU
2011 – 2016	Head of the Computer Architecture and Design (CARD) Research Group, Dept. of Computer and Information Science, NTNU
2013 – 2016	Coordinator of the Energy Efficient Computing Systems (EECS) faculty research initiative

7 Teaching Activities

7.1 Courses

Spring 2021	Lecturer (one lecture)	DT8123 Advanced Computing
Autumn 2020	Lecturer and Coordinator	TDT4255 Computer Design
Autumn 2019	Lecturer and Coordinator	TDT4255 Computer Design
Autumn 2019	Lecturer	TDT1 Architecture of Computer Systems
Spring 2019	Coordinator	DT8105 Computer Architecture 2
Autumn 2018	Coordinator	TDT4295 Computer Design Project
Autumn 2018	Lecturer and Coordinator	TDT4255 Computer Design
Spring 2016	Coordinator	DT8105 Computer Architecture 2
Autumn 2016	Coordinator	TDT1 Architecture of Computer Systems
Autumn 2016	Coordinator	TDT4295 Computer Design Project
Autumn 2016	Coordinator	TDT4255 Computer Design
Autumn 2015	Coordinator	TDT4258 Energy Efficient Computer Systems
Autumn 2015	Coordinator	TDT4255 Computer Design
Spring 2015	Coordinator	TDT4258 Energy Efficient Computer Systems
Autumn 2014	Coordinator	TDT4255 Computer Design
Spring 2014	Coordinator	TDT4258 Energy Efficient Computer Systems
Autumn 2013	Lecturer and Coordinator	TDT4255 Computer Design
Spring 2013	Coordinator	TDT4258 Energy Efficient Computer Systems
Autumn 2012	Lecturer and Coordinator	TDT4255 Computer Design
Autumn 2012	Coordinator	TDT4295 Computer Design Project
Spring 2012	Lecturer and Coordinator	TDT4260 Computer Architecture
Autumn 2011	Lecturer and Coordinator	TDT4255 Computer Design
Autumn 2011	Coordinator	TDT4295 Computer Design Project
Autumn 2011	Coordinator	TDT1 Energy Efficient Multi-core Computing
Spring 2011	Lecturer and Coordinator	TDT4258 Microcontroller Systems Design
Autumn 2010	Lecturer and Coordinator	TDT4160 Computer Fundamentals
Autumn 2010	Coordinator	TDT4295 Computer Design Project
Autumn 2010	Lecturer	TDT4260 Computer Architecture

7.2 Supervised Master Students

Summary: I have supervised 24 master students.

2020	Towards Efficiently Utilizing Coarse-Grained Reconfigurable Accelerators	Lasse Agentoft Eggen
2020	Minimizing the Energy Consumption of Soft Real-Time Applications on a Multi-Core Ultra-Low-Power Device	Eirik Vale Aase
2020	Accelerating Object Detection for Agricultural Robotics	Jørgen Boganes
2020	Predicting Interference-Free Performance with Linear Model Trees	Peter Salvesen
2020	Fast Call Graph Profiling	Eirik Smithsen
2017	Evaluating Shared Last Level Cache Partitioning Algorithms	Thomas Alexander aan de Wiel
2017	Vectorized Benchmarks for the Berkeley Dwarfs	Christian De Frene
2017	Extending OMPT to Support Grain Graph Visualization	Peder Voldnes Langdal
2017	Pre-processing of Graphs	Anders Sildnes
2016	Designing a Virtual Memory System for the SHMAC Research Infrastructure	Audun Sutterud
2015	Evaluation of Cache Management Algorithms for Shared Last Level Caches	Runar Bergheim Olsen
2014	Design and Implementation of a High-Performance Processor Core for the Heterogeneous SHMAC Multi-Core Prototype	Anders Akre and Sebastian Tvetmarken Bøe
2014	Task Based Parallel Programming on the SHMAC Multi-Core Prototype	Magnus Walstad
2014	Implementing a bare-metal threading library for SHMAC	Håkon Opsvik Wikene
2013	Improving Energy Efficiency with Special-Purpose Accelerators	Alexandru Fiodorov
2013	A Comparative Analysis of Shared Cache Management Techniques for Chip Multiprocessor	Christian Grøvdal
2013	A Cycle-accurate Simulation Infrastructure for the Heterogeneous SHMAC Multi-Core Prototype	Yaman Umuroglu
2012	Saving Energy in Periodic Embedded Systems with Memory System Techniques (with Nordic Semiconductor)	Stian Fredrikstad
2012	Towards Energy-Efficient Hardware Acceleration of Embedded GPU Drivers (with ARM)	Ole Magnus Ruud and Vegar Kåsli
2012	Implementing a Heterogeneous Multi-Core Prototype in an FPGA **(Best FPGA master thesis award)**	Leif Tore Rusten and Gunnar Inge Sortland
2011	Multi-Processor System-on-Chip Architectures for Wireless Applications (with Nordic Semiconductor)	Anders Nore

7.3 Other Teaching Activities

2015	Jury member for the Norwegian Computing Center prize for best master thesis within computer science and mathematics
2014	Educational training for academic staff (PEDUP) (100 hours)
2011-2012	Project Manager, Fremtidens IKT-utdanning (FRIKT), Subproject “Computer Science”
2011	Project Manager, Fremtidens IKT-utdanning (FRIKT), Subproject “Basic Education”

8 Research Activities

Summary:
H-index: 13. i10-index: 22. Total number of citations: >1050. >45 peer-reviewed publications including top-tier international venues such as ISCA, MICRO, HPCA, and ASPLOS.

8.1 Research Projects

Time	Role	Name	Funding
2020-2023	Scientific advisor	Boosting Widening Digital Innovation Hubs (BOWI)	EU H2020, ICT-01-2019, overall budget 8.0 MEUR, NTNU grant 285 kEUR.
2020-2020	Scientific advisor	Drill String Dynamics	1 MNOK from NTNU Discovery
2019-2023	Project Manager and PI	Balancing Compute and Memory Performance in Reconfigurable Accelerators with Analytical Modeling (BAMPAM)	7.8 MNOK from the Norwegian Research Council, 1.3 MNOK own funding from NTNU
2019-2019	Principal Investigator	Non-Intrusive Power Monitor for Low-Energy Computing Systems (NIPOLECS)	26 kEUR from TETRAMAX (total budget 44 kEUR)
2017-2018	Principal Investigator	Reducing Power Consumption in Microprocessors (RPCM)	500 KNOK from the Regional Research Fund for Mid-Norway
2017-2020	Project Manager and PI	Energy efficient high Performance computing research InfrastruCture (EPIC)	3 MNOK from NTNU
2016-2019	WP Leader	Towards Ubiquitous Low-power Image Processing Platforms (TULIPP)	EU H2020, ICT4.b-2015, budget 4.7 Million EUR, NTNU grant 696 000 EUR
2015-2018	Principal Investigator	Run-time Exploitation of Application Dynamism for Energy-efficient Exascale computing (READEX)[1]	EU H2020, FETHPC-1-2014, budget 3.5 Million EUR, NTNU grant 700 000 EUR
2013-2019	Principal Investigator	ARM-CARD Lab	Funded by ARM: One lecturer/researcher at post doc level
2013-2018	Project Manager	Single-ISA Heterogeneous MAny-core Computer (SHMAC)	Funded by NTNU
2013-2014	Principal Investigator	Vectorized PARSEC Benchmarks (ParVec)	Funded by NTNU: 1 post doc.

[1] READEX was ranked as number 1 (79 evaluated proposals) with score 14.0 (maximum 15.0)

8.2 Supervision and Mentoring

- Formal main supervisor of 6 PhD students out of which 2 have graduated.
- Formal co-supervisor of 7 PhD students out of which 2 have graduated.
- Mentor of 5 post-doctoral researchers.

Current:

2020 – present	Lasse Agentoft Eggen	Main Supervisor
2020 – present	Anders Gaustad	Formal co-supervisor
2020 – present	Fatemeh Ghasemi	Main Supervisor
2020 – present	Amund Bergsland Kvalsvik	Formal co-supervisor
2019 – present	Joseph Rogers	Main Supervisor
2018 – present	Björn Gottschall	Main Supervisor
2019 – present	Truls Asheim	Formal co-supervisor
2017 – present	Lahiru Rasnayake	Formal co-supervisor
2013 – present	Even Låte	Formal co-supervisor

Alumni:

	Name	**My role**	**Next employer**
2013 – 2019	Dr. Asbjørn Djupdal	Mentoring	NTNU
2012 – 2019	Dr. Nico Reissman	Main Supervisor	NTNU
2012 – 2018	Dr. Yaman Umuroglu	Main Supervisor	Xilinx
2012 – 2018	Dr. Yahya Yassin	Formal co-supervisor	Mode Sensors
2016 – 2018	Dr. Ananya Muddukrishna	Mentoring	ÅF
2015 – 2017	Dr. Mohammed Sourouri	Mentoring	Accenture
2012 – 2017	Dr. Odd Rune Strømmen Lykkebø	Formal co-supervisor	Nnaisense
2013 – 2014	Dr. Nikita Nikitin	Mentoring	Mentor Graphics
2012 – 2014	Dr. Juan Manuel Cebrian	Mentoring	UPC/BSC

8.3 International Peer-Reviewed Journal Publications

13. Fast and Accurate Edge Computing Energy Modeling and DVFS Implementation in GEM5 using System Call Emulation Mode
Yahya Yassin, *Magnus Jahre*, Per Gunnar Kjeldsberg, Snorre Aunet, and Franky Catthoor
In: Journal of Signal Processing Systems, 2020

12. DCMI: A Scalable Strategy for Accelerating Iterative Stencil Loops on FPGAs
Mostafa Koraei, Omid Fatemi, and *Magnus Jahre*
In: ACM Transactions on Architecture and Code Optimization, 2019

11. Modeling Emerging Memory-Divergent GPU Applications
Lu Wang, *Magnus Jahre,* Almutaz Adileh, Zhiying Wang, and Lieven Eeckhout
In: Computer Architecture Letters, 2019

10. Scalability Analysis of AVX-512 Extensions
Juan M. Cebrian, Lasse Natvig, and *Magnus Jahre*
In: Journal of Supercomputing, 2019

9. The READEX Formalism for Automatic Tuning for Energy Efficiency
Joseph Schuchart, Michael Gerndt, Per Gunnar Kjeldsberg, Michael Lysaght, David Horák, Lubomír Říha, Andreas Gocht, Mohammed Sourouri, Madhura Kumaraswamy, Anamika Chowdhury, *Magnus Jahre*, Kai Diethelm, Othman Bouizi, Umbreen Sabir Mian, Jakub Kruzík, Radim Sojka, Martin Beseda, Venkatesh Kannan, Zakaria Bendifallah, Daniel Hackenberg and Wolfgang E. Nagel
In: Computing, 2017

8. Random Access Schemes for Efficient FPGA SpMV Acceleration
Yaman Umuroglu and *Magnus Jahre*
In: Microprocessors and Microsystems, 2016

7. Tuning the Victim Selection Policy of Intel TBB
Alexandru C. Iordan, *Magnus Jahre* and Lasse Natvig
In: Journal of Systems Architecture, Volume 61, Issue 10, 2015

6. ParVec: Vectorizing the PARSEC Benchmark Suite
Juan M. Cebrian, *Magnus Jahre* and Lasse Natvig
In: Computing, 2015

5. Perfect Reconstructability of Control Flow from Demand Dependence Graphs
Helge Bahmann, Nico Reissmann, *Magnus Jahre* and Jan Christian Meyer
In: ACM Transactions on Architecture and Code Optimization, 2015

4. Storage Efficient Hardware Prefetching using Delta Correlating Prediction Tables
Marius Grannæs, *Magnus Jahre* and Lasse Natvig
In: Journal of Instruction Level Parallelism, Volume 13, 2011

3. Multi-Level Hardware Prefetching using Low Complexity Delta Correlating Prediction Tables with Partial Matching
Marius Grannæs, *Magnus Jahre* and Lasse Natvig
In: Transactions on High-Performance Embedded Architectures and Compilers, 2011

2. A High Performance Adaptive Miss Handling Architecture for Chip Multiprocessors
Magnus Jahre and Lasse Natvig
In: Transactions on High-Performance Embedded Architectures and Compilers, Volume 4, Issue 1, 2009

1. Experimental Validation of the Learning Effect for a Pedagogical Game on Computer Fundamentals
Guttorm Sindre, Lasse Natvig and *Magnus Jahre*
In: IEEE Transactions on Education, 2009

8.4 International Peer-Reviewed Conference and Workshop Publications

35. MDM: The GPU Memory Divergence Model
Lu Wang, *Magnus Jahre*, Almutaz Adileh, and Lieven Eeckhout
In: International Symposium on Microarchitecture (MICRO), 2020

34. Selective Replication in Memory-Side GPU Caches
Xia Zhao, *Magnus Jahre*, and Lieven Eeckhout
In: International Symposium on Microarchitecture (MICRO), 2020

33. HSM: A Hybrid Slowdown Model for Multitasking GPUs
Xia Zhao, *Magnus Jahre*, and Lieven Eeckhout
In: International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2020

32. Finger Finder: A Low-Energy Peak Detection Accelerator for Capacitive Touch Controllers
Kai Kristian Amundsen, Gaute Myklebust, Per Gunnar Kjeldsberg, and *Magnus Jahre*
In: Third Workshop on Computer Architecture Research with RISC-V (CARRV), 2019

31. Get Out of the Valley: Power-Efficient Address Mapping for GPUs
Yuxi Liu, Xia Zhao, *Magnus Jahre,* Zhenlin Wang, Xiaolin Wang, Yingwei Luo and Lieven Eeckhout
In: International Symposium on Computer Architecture (ISCA), 2018

30. Supporting Utilities for Heterogeneous Embedded Image Processing Platforms (STHEM): An Overview
Ahmad Sadek, Ananya Muddukrishna, Lester Kalms, Asbjørn Djupdal, Ariel Podlubne, Antonio Paolillo, Diana Goehringer and *Magnus Jahre*
In: International Symposium on Applied Reconfigurable Computing (ARC), 2018

29. GDP: Using Dataflow Properties to Accurately Estimate Interference-Free Performance at Runtime
Magnus Jahre and Lieven Eeckhout
In: International Symposium on High-Performance Computer Architecture (HPCA), 2018

28. Aggregating Large Grain Graphs for Improved OpenMP Productivity
Nico Reissmann, *Magnus Jahre* and Ananya Muddukrishna
In: Fourth International Workshop on Visual Performance Analysis (VPA), 2017

27. Streamlined Deployment for Quantized Neural Networks
Yaman Umuroglu and *Magnus Jahre*
In: International Workshop on Highly Efficient Neural Networks Design (HENND), 2017

26. Extending OMPT to Support Grain Graphs
Peder Voldnes Langdal, *Magnus Jahre* and Ananya Muddukrishna
In: 13th International Workshop on OpenMP (IWOMP), 2017

25. Towards Efficient Quantized Neural Network Inference on Mobile Devices
Yaman Umuroglu and *Magnus Jahre*
In: International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), 2017

24. Enabling Exhaustive Exploration of FPGA Temporal Partitions for Streaming HPC Applications
Mostafa Koraei, *Magnus Jahre* and S. Omid Fatemi
In: International Symposium on Highly-Efficient Accelerators and Reconfigurable Technologies (HEART), 2017

23. Scaling Binarized Neural Networks on Reconfigurable Logic
Nicholas J. Fraser, Yaman Umuroglu, Giulio Gambardella, Michaela Blott, Philip Leong, *Magnus Jahre* and Kees Vissers
In: 8th Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures and 6th Workshop on Design Tools and Architectures for Multicore Embedded Computing Platforms (PARMA-DITAM), 2017

22. FINN: A Framework for Fast, Scalable Binarized Neural Network Inference
Yaman Umuroglu, Nicholas J. Fraser, Giulio Gambardella, Michaela Blott, Philip Leong, *Magnus Jahre* and Kees Vissers
In: Proceedings of the ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA), 2017

21. Towards Efficient Design Space Exploration of FPGA-based Accelerators for Streaming HPC Applications
Mostafa Koraei, *Magnus Jahre* and S. Omid Fatemi
In: Proceedings of the ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA), 2017

20. Studying Data Forwarding on a Non-Coherent Tiled Multicore
Asbjørn Djupdal, *Magnus Jahre* and Magnus Själander
In: Nordic Workshop on Multi-core Computing (MCC), 2016

19. Efficient Control Flow Restructuring for GPGPU Programs
Nico Reissmann, Thomas L. Falch, Benjamin A. Bjørnseth, Helge Bahmann, Jan Christian Meyer and *Magnus Jahre*
In: International Conference on High Performance Computing & Simulation (HPCS), 2016
(Outstanding Paper Award)

18. TULIPP: Towards Ubiquitous Low-power Image Processing Platforms
Tobias Kalb, Lester Kalms, Diana Göhringer, Carlota Pons, Fabien Marty, Ananya Muddukrishna, *Magnus Jahre*, Per Gunnar Kjeldsberg, Boitumelo Ruf, Igor Tchouchenkov, Carl Ehrenstråhle, Magnus Peterson, Flemming Christensen, Antonio Paolillo, Christian Lemer, Ben Rodriguez, Guillaume Bernard, Francois Duhem and Philippe Millet
In: International Conference on Embedded Computer Systems: Architectures, Modelling and Simulation (SAMOS), 2016

17. Hybrid Breadth-First Search on a Single-Chip FPGA-CPU Heterogeneous Platform
Yaman Umuroglu, Donn Morrison and *Magnus Jahre*
In: 25th International Conference on Field-programmable Logic and Applications (FPL), 2015

16. A Vector Caching Scheme for Streaming FPGA SpMV Accelerators
Yaman Umuroglu and *Magnus Jahre*
In: The 11th International Symposium on Applied Reconfigurable Computing (ARC), 2015

15. An Energy Efficient Column-Major Backend for FPGA SpMV Accelerators
Yaman Umuroglu and *Magnus Jahre*
In: The 32nd International Conference on Computer Design (ICCD), 2014

14. Graph-based Performance Accounting for Chip Multiprocessor Memory Systems
Magnus Jahre
In: The 23rd International Conference on Parallel Architectures and Compilation Techniques (PACT), 2014

13. Patterned Heterogeneous CMPs: The Case for Regularity-Driven System-Level Synthesis
Nikita Nikitin and *Magnus Jahre*
In: IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2014

12. A Study of Energy and Locality Effects Using Space-filling Curves
Nico Reissmann, Jan Meyer, and *Magnus Jahre*
In: The Tenth Workshop on High-Performance, Power-Aware Computing (HPPAC), 2014

11. Optimized Hardware for Suboptimal Software: The Case for SIMD-aware Benchmarks
Juan M. Cebrián, *Magnus Jahre* and Lasse Natvig
In: International Symposium on Performance Analysis of Systems and Software (ISPASS), 2014

10. Victim Selection Policies for Intel TBB: Overheads and Energy Footprint
Alexandru C. Iordan, *Magnus Jahre*, Lasse Natvig
In: Architecture of Computing Systems (ARCS). 2014

9. Challenges of Reducing Cycle-Accurate Simulation Time for TBP Applications
Alexandru C. Iordan, *Magnus Jahre* and Lasse Natvig
In: Procedia Computer Science 2013; Volume 18, 2013

8. On the Energy Footprint of Task Based Parallel Applications
Alexandru C. Iordan, *Magnus Jahre* and Lasse Natvig
In: Proceedings of the 2013 International Conference on High Performance Computing & Simulation (HPCS), 2013

7. Exploring the Prefetcher/Memory Controller Design Space: An Opportunistic Prefetch Scheduling Strategy
Marius Grannæs, *Magnus Jahre* and Lasse Natvig
In: Architecture of Computing Systems (ARCS), 2011

6. DIEF: An Accurate Interference Feedback Mechanism for Chip Multiprocessor Memory Systems
Magnus Jahre, Marius Grannæs and Lasse Natvig
In: The 5th International Conference on High Performance and Embedded Architectures and Compilers, 2010

5. Multi-Level Hardware Prefetching using Low Complexity Delta Correlating Prediction Tables with Partial Matching
Marius Grannæs, *Magnus Jahre* and Lasse Natvig
In: The 5th International Conference on High Performance and Embedded Architectures and Compilers, 2010
(Nominated for Best Paper Award)

4. A Quantitative Study of Memory System Interference in Chip Multiprocessor Architectures
Magnus Jahre, Marius Grannæs and Lasse Natvig
In: 11th IEEE International Conference on High Performance Computing and Communications (HPCC), 2009

3. A Light-Weight Fairness Mechanism for Chip Multiprocessor Memory Systems
Magnus Jahre and Lasse Natvig
In: ACM International Conference on Computing Frontiers, 2009

2. Storage Efficient Hardware Prefetching using Delta Correlating Prediction Tables
Marius Grannæs, *Magnus Jahre* and Lasse Natvig
In: 1st JILP Data Prefetching Championship, 2009

1. Low-Cost Open-Page Prefetch Scheduling in Chip Multiprocessors
Marius Grannæs, *Magnus Jahre* and Lasse Natvig
In: XXVI IEEE International Conference on Computer Design (ICCD), 2008

8.5 Other Publications

7. Challenges in the Realm of Embedded Real-Time Image Processing
Philippe Millet, Michael Grinberg, and *Magnus Jahre*
In: Jahre M., Göhringer D., Millet P. (eds) Towards Ubiquitous Low-power Image Processing Platforms. Springer, 2012

6. TRP: A Foundational Platform for High-Performance Low-Power Embedded Image Processing
Magnus Jahre and Philippe Millet
In: Jahre M., Göhringer D., Millet P. (eds) Towards Ubiquitous Low-power Image Processing Platforms. Springer, 2012

5. STHEM: Productive Implementation of High-Performance Embedded Image Processing Applications
Magnus Jahre
In: Jahre M., Göhringer D., Millet P. (eds) Towards Ubiquitous Low-power Image Processing Platforms. Springer, 2012

4. Lynsyn and LynsynLite: The STHEM Power Measurement Units
Asbjørn Djupdal, Björn Gottschall, Fatemeh Ghasemi, and *Magnus Jahre*
In: Jahre M., Göhringer D., Millet P. (eds) Towards Ubiquitous Low-power Image Processing Platforms. Springer, 2012

3. Developing Low-Power Image Processing Applications with the TULIPP Reference Platform Instance
Tobias Kalb, Lester Kalms, Diana Göhringer, Carlota Pons, Ananya Muddukrishna, *Magnus Jahre*, Boitumelo Ruf, Tobias Schuchert, Igor Tchouchenkov, Carl Ehrenstråhle, Magnus Peterson, Flemming Christensen, Antonio Paolillo, Ben Rodriguez and Philippe Millet
In: Hardware Accelerators in Datacenters, Eds. Christoforos Kachris, Babak Falsafi and Dimitrios Soudris, Springer, 2018

2. Towards Efficient Simulation of Task Based Parallel Applications
Alexandru C. Iordan, *Magnus Jahre* and Lasse Natvig
In: Norwegian Informatics Conference (NIK), 2012

1. Performance Effects of a Cache Miss Handling Architecture in a Multi-core Processor
Magnus Jahre and Lasse Natvig
In: Norwegian Informatics Conference (NIK), 2007

8.6 Books

1. Towards Ubiquitous Low-power Image Processing Platforms
Magnus Jahre, Diana Göhringer and Philippe Millet (Editors)
Springer Nature, 2021

8.7 Commissions of Trust

2022	**International Symposium on High-Performance Computer Architecture (HPCA)**	**PC Member**
2021	IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)	Reviewer
2021	International Symposium on Computer Architecture (ISCA)	External Review Committee (ERC)
2020	International Symposium on Microarchitecture (MICRO)	External Review Committee (ERC)
2020	**International Symposium on Computer Architecture (ISCA)**	**PC Member**
2020	Programmability and Architectures for Heterogeneous Multicores (MULTIPROG)	PC Member
2020	IEEE Transactions on Computers (TC)	Reviewer
2020	ACM Transactions on Embedded Computing Systems (TECS)	Reviewer
2019	12th Nordic Workshop on Multi-core Computing (MCC)	PC Member
2019	Journal of Supercomputing	Reviewer
2019	ACM SIGPLAN/SIGBED Conference on Languages, Compilers, Tools and Theory for Embedded Systems (LCTES)	PC Member
2019	IEEE Transactions on Computers	Reviewer
2018	Eleventh Nordic Workshop on Multi-core Computing (MCC)	PC Member
2018	Journal of Parallel and Distributed Computing (JPDC)	Reviewer
2018	ACM SIGPLAN/SIGBED Conference on Languages, Compilers, Tools and Theory for Embedded Systems (LCTES)	PC Member
2018	Euromicro International Conference on Parallel, Distributed and Network-based Processing (PDP)	PC Member
2017	IEEE Transactions on Computers	Reviewer
2017	Research Foundation - Flanders (Fonds Wetenschappelijk Onderzoek - Vlaanderen, FWO)	Reviewer
2017	ACM Transactions on Architecture and Code Optimization (TACO)	Reviewer
2017	Euromicro International Conference on Parallel, Distributed and Network-based Processing (PDP)	PC Member

2016	**Ninth Nordic Workshop on Multi-core Computing (MCC)**	**General Chair**
2016	ACM Transactions on Architecture and Code Optimization (TACO)	Reviewer
2016	Workshop on Many-core Embedded Systems (MES) @ ISCA	PC Member
2016	SpringerPlus Journal	Reviewer
2016	Microprocessors and Microsystems (MICPRO) Journal	Reviewer
2016	Computer Science Review (COSREV) Journal	Reviewer
2016	Euromicro International Conference on Parallel, Distributed and Network-based Processing (PDP)	PC Member
2015	Journal of Signal Processing Systems	Reviewer
2015	ACM Transactions on Architecture and Code Optimization (TACO)	Reviewer
2015	Workshop on Many-core Embedded Systems (MES) @ ISCA	PC Member
2015	Euromicro International Conference on Parallel, Distributed and Network-based Processing (PDP)	PC Member
2014	ACM Transactions on Embedded Computing Systems (TECS)	Reviewer
2014	Journal of Signal Processing Systems	Reviewer
2014	International Symposium on Computing and Networking (CANDAR)	PC Member
2014	Workshop on Many-core Embedded Systems (MES) @ ISCA	PC Member
2013	International Symposium on Computing and Networking (CANDAR)	PC Member
2012	International Conference on Networking and Computing (ICNC)	PC Member
2011	IEEE Transactions on Parallel and Distributed Systems	Reviewer
2011	Workshop on Highly Parallel Processing on a Chip (HPCC)	PC Member
2011	International Conference on Networking and Computing (ICNC)	PC Member
2011	International Conference on Computing Frontiers	Reviewer
2010	Workshop on Highly Parallel Processing on a Chip (HPCC)	PC Member

8.8 Evaluation Committees

2020	PhD opponent, Lu Wang, Ghent University, Belgium
2019	PhD opponent, Xia Zhao, Ghent University, Belgium
2019	Second PhD opponent, Vi Tran, University of Tromsø, Norway
2018	PhD opponent, Sander De Pestel, Ghent University, Belgium
2018	Opponent for Licentiate thesis, Alexandra Angerd, Chalmers, Sweden
2017	Administrator of the evaluation committee for a tenure-track associate professor position in Computer Architecture, NTNU
2017	Employee representative in the evaluation committee for the Head of Department position, Dept. of Computer Science, NTNU
2015	Internal member of the evaluation committee for an associate professor position in Computer Architecture, NTNU
2014	External PhD thesis reviewer, Syed Jafri, University of Turku, Finland

8.9 Invited Talks

2018	*"Get Out of the Valley: Power-Efficient Address Mapping for GPUs",* Chalmers University of Technology, Gothenburg, Sweden
2017	*"Using FPGAs to Accelerate Neural Network Inference",* RC4DL: Reconfigurable Computing for Deep Learning, Workshop at the 27th International Conference on Field-Programmable Logic and Applications (FPL), Ghent, Belgium
2017	*"Multi-core Memory System Resource Management and Accelerators",* PerformanceLab, Ghent University, Belgium

2016	*"Climbing the Complexity Wall with Efficient Tools and Abstractions"*, University of Tromsø, Norway
2011	*"Multi-core Memory System Resource Management"*, Multi-core Day, Swedish Institute of Computer Science (SICS), Stockholm, Sweden
2010	*"Multi-core Memory Systems: Research Results, Methods and Future Plans"*, ARM ERSC, Cambridge, UK

8.10 Miscellaneous

- Session chair "Memory Compression" within the paper track at HiPEAC 2018

9 Popular Science and User-oriented Dissemination

2020	*"Hvor klimafarlig er internett? Datasentre står for 1 prosent av verdens energibruk, ifølge ny studie.", Interview, Forskning.no*	Newspaper
2019	Interview, Frokostradioen, NRK P1+	Radio
2017	*"Dette er det første du må gjøre i dag: Oppdater datamaskinen", Interview, VG 15/5-17 and vg.no*	Newspaper
2017	*"Ein æra er omme",* Interview, nrk.no	Newspaper
2016	*"The Norwegian Microelectronics Industry"*, NHO visit to NTNU	Presentation
2016	*"Blir PC-en og mobilen tregere med årene?",* Interview, Aftenposten	Newspaper
2016	*"Productivity vs. Efficiency: Harnessing the Compute Power of Current and Future Parallel Computer Architectures",* Workshop with Norwegian industry in relation to the KID industry network.	Workshop
2015	*"Fremtidens superdatamaskiner må være energieffektive"*, NTNU Tech Zone	Blog
2015	Green ICT presentation at Heimdal upper secondary school in relation to the EU-project "Use IT Smartly".	Presentation
2014	Interview, Nyhetslunsj, NRK P2	Radio
2014	*"Kaster bort strøm for milliarder",* Dagens Næringsliv, **(front page)**	Newspaper
2014	*«Energy Efficient Computing Systems»,* Centre for the Development of Industrial Technology (CDTI) visit at NTNU	Presentation
2014	*«Energy Efficient Computing Systems»,* NxtMedia board visit at NTNU	Presentation
2013	*"Hvordan datateknologien redder verden",* IT-camp for jenter	Presentation
2013	*"Teknisk sett: 5 spørsmål om grønn IT"*, Teknisk Ukeblad	Newspaper
2013	*"Effektiv Elektronikk"*, Dagens Næringsliv	Newspaper
2013	*"Forskningsfyrtårnet NTNU Energy Efficient Computing Systems (EECS)"*, Elektronikk: Tidsskrift for IT og Telekom	Magazine
2012	*"Hvordan datateknikken redder verden"*, IT-camp for jenter	Presentation
2011	*"Computational Computer Architecture"*, Meta	Magazine
2010	*"Computational Computer Architecture Research at NTNU"*, ERCIM News	Magazine