Address: H0201, Gamle Jonsvannsveien 125
7048 Trondheim, Norway
Mobile: +47 4658 3197
e-mail: shou46@gmail.com

Dr. Shounak Chakraborty

Current Position

I am a **Researcher** working with **Prof. Magnus Själander** at the **Dept. of Computer Science, NTNU, Trondheim, Norway** since January 1, 2023, where I also worked as a **Post Doctoral Fellow (through ERCIM and Marie Curie Individual Fellowship (MSCA-IF))**, since January 1, 2019. Primarily, my broad research area is **Computer Architecture**, where specifically, I work towards improving **Energy & Thermal Efficiencies** of homogeneous as well as heterogeneous Chip Multi-Processors. Since June 2022, I am also working as a **Computer System Architect** with **ZeroPoint Technologies AB**, Gothenburg, Sweden.

My Erdős Number is currently 4.

Personal Information

Chakraborty, Shounak
Date of birth: 09-November-1987
Sex: Male
Nationality: Indian
ORCID: 0000-0003-1679-6210
URL for personal website: https://www.ntnu.edu/employees/shounakc
URL for LinkedIn: https://www.linkedin.com/in/shounak-chakraborty-2b829417

Education

Doctor of Philosophy (Computer Sc. & Engineering) December 2011 – February 2018
Indian Institute of Technology Guwahati, Guwahati, India

- Thesis Supervisor: Prof. Hemangee Kalpesh Kapoor
- Title of Thesis: Energy and Thermal Management of CMPs by Dynamic Cache Reconfiguration
- Defended on: February 22, 2018

Master of Engineering (Computer Sc. & Engineering) August 2009 – July 2011
College of Engineering Guindy, Anna University, Chennai, India

- CPI: 7.85/10

Bachelor of Technology (Computer Sc. & Engineering) August 2005 – June 2009
MCKV Institute of Engineering, Howrah, India (Affiliation: MAKAUT, formerly known as WBUT)

- CGPA: 8.01/10

Higher Secondary Examinations July 2003 – June 2005
Anandamath Vidyapith (WBCHSE), West Bengal, India

- Marks Percentage: 77.4%

Secondary Examination June 2003
Bhogpur K.M. High School (WBBSE), West Bengal, India

- Marks Percentage: 76.6%

Work Experiences

- Designation : Researcher at the Department of Computer Science,
  Research Focus: Energy & Thermal Efficiency, NVMs, Caches & Cores.
  Organization: Norwegian University of Science & Technology (NTNU), Trondheim, Norway.
  Duration: January 1, 2023, to *till date*.

- Designation : Computer System Architect,
  Organization: ZeroPoint Technologies AB, Gothenburg, Sweden.
  Duration: June 1, 2022, to *till date*.

- Designation : Marie Curie Post Doctoral Fellow (MSCA-IF),
  Research Focus: Energy & Thermal Efficiency, NVMs, Caches & Cores.
  Organization: Norwegian University of Science & Technology (NTNU), Trondheim, Norway.
  Duration: January 1, 2021, to December 31, 2022.

- Designation : ERCIM Post Doctoral Fellow,
  Research Focus: Caches & Cores, Energy & Thermal Efficiency.
  Organization: Norwegian University of Science & Technology (NTNU), Trondheim, Norway.
  Duration: January 1, 2019, to December 31, 2020.

- Designation : Assistant Professor,
  Organization: Indian Institute of Information Technology Guwahati, Guwahati, Assam, India.
  Duration: July 2018 to December 2018.
  Courses: Compilers (UG), Compiler Lab (UG)

- Designation : Teaching Assistant (During Ph.D.),
  Organization: Indian Institute of Technology Guwahati, India.
  Duration: December 2011 to June 2017.
  Courses: *(1) UG Courses-* Computer Architecture & Organization (Once), Introduction to Computing (Twice), Digital Design (Twice), Programming Lab (Once), Microprocessor Lab (Once); *(2) PG Courses-* Advanced Computer Architecture (Twice), Parallel Computer Architecture (Once)
- Designation : Assistant Professor,
  Organization: Future Institute of Engineering & Management, Kolkata, West Bengal, India.
  Duration: July 2011 to December 2011.
  Courses: Compiler Design (UG), DBMS (UG)

Awards

- Received **Marie Skłodowska-Curie Actions-Individual Fellowship (MSCA-IF)** from European Commission for **Post Doctoral Research at NTNU, Trondheim, Norway**

  Project Title: TECTONIC (Towards Employing Compilers for Thermal Management and Optimal Data Placement in Hybrid Cache)

  Duration: 24 months (January 1, 2021, to December 31, 2022)

  Amount: EUR 214,158.72
- Selected in "**ERCIM Alain Bensoussan Fellowship Programme**" (supported by the FP7 Marie Curie Actions) of the European Commission for doing **Post Doctoral Research at NTNU, Trondheim, Norway** (From January 1, 2019 to December 31, 2020).
- Received travel grant for attending **VLSI Design 2017** at Hyderabad, India.
- Received travel grant from **Student Travel Award Program of ACM-SIG** for attending **ACM SAC 2016** at Pisa, Italy.
- Received travel grant from **IFIP/IEEE** for attending **VLSI SoC 2016** at Tallinn, Estonia.
- Received student travel grant for attending **IPDPS 2015** at Hyderabad, India.
- Received **MHRD Scholarship, Govt. of India** for 5 years during PhD at IIT Guwahati, India.
- Received **MHRD Stipend, Govt. of India** for 2 years Masters study at College of Engineering Guindy, Anna University Chennai, India by qualifying **GATE 2009 in Computer Science, with All India Rank 874 out of 43170 candidates**.

Supervisions

- Co-supervisor (remotely): Y. Sharma, Ph.D. Scholar, IIIT Guwahati, India (2020-)
- Co-supervisor (remotely): Z. Das, B.Tech, IIIT Guwahati, India (2020-21)
- Main supervisor: M. Srikant, B.Tech, IIIT Guwahati, India (2018-19)

Invited Talk/Seminar/ Lecture

- Presented: "WaFFLe: Gated Cache-Ways with Per-core Fine-grained DVFS for Reduced On-chip Temperature and Leakage Consumption" (published in ACM TACO, December 2021) at **HiPEAC 2022 Conference, Budapest, Hungary** during June 20-22, 2022.
- Delivered Online Lecture on: "Computer Systems Engineering: What to explore & Why?" at **Universidad Politécnica de Texcoco, Mexico** on November 13, 2020.
- Delivered lectures (through TEQIP) on: "Real-Time Systems: A Computer Architecture Perspective" at **IIIT Guwahati, Guwahati, India** during September 12-14, 2020.
- Webinar Seminar: "Modern Computation: Energy vs. Performance" at **VIT, Vellore, India** on June 26, 2020.
- Webinar Seminar: "Modern Computation: Energy vs. Performance" at **Hindustan University, Chennai, India** on May 25, 2020.

- "TECTONIC: Towards Employing Compilers for Thermal Management and Optimal Data Placement in Hybrid Cache" at **ARM Research Summit 2019, Texas, USA** during September 15-18, 2019.
- Delivered talk on "Energy and Thermal Management of CMPs" at **Dept. of CSE, IIT Delhi, India** on May 8, 2018.

Project Management Experience

- **Title:** "TECTONIC: Towards Employing Compilers for Thermal Management and Optimal Data Placement in Hybrid Cache"
  Duration: January 2021 - December 2022
  Source of funding and amount: MSCA-IF (EU), EUR 214,158.72
  Status: Ongoing

Research Interests

My research interest currently focuses on the following areas of Modern Computer Architecture-

- Energy & Thermal Efficiencies
- Emerging Memory Technologies
- Caches and Cores
- SoC Design

I am also interested to expand the boundaries of my work between Application, Operating System, Compilers and Hardware.

Major Collaborations

- Prof. Klaus McDonald-Maier, University of Essex, UK. (2020 - present)
- Dr. Sangeet Saha, University of Essex, UK. (2020 - present)
- Dr. Sukarn Agarwal, University of Edinburgh, UK. (2020 - present)
- Prof. David Whalley, Florida State University, USA (2022 - present)
- Prof. (Late) Vassos Soteriou, Cyprus University of Technology, Cyprus. (2019 - 2020)
- Dr. Sanjay Moulik, IIIT Guwahati, India. (2018 - present)
- Dr. Rajesh D., NVIDIA. (2018 - present)
- Prof. Rishad Shafique, Newcastle University, UK. (2021 - present)

Publications

Journals

- S. Saha, **S. Chakraborty**, S. Agarwal, R. Gangopadhyay, M. Själander, and K. D. McDonald-Maier, "DELICIOUS: Deadline-Aware Approximate Computing in Cache-Conscious Multicore"- *IEEE Transactions on Parallel and Distributed Systems **[TPDS]***, (accepted on December 4, 2022) [in press].
- S. Saha, **S. Chakraborty**, X. Zhai, S. Ehsan, and K. D. McDonald-Maier, "ACCURATE: Accuracy Maximization for Real-Time Multi-core systems with Energy Efficient Way-sharing Caches"-*IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems **[TCAD]***, Vol. 41, Issue 12, December 2022, Pages: 5246-5260.
- Y. Sharma, **S. Chakraborty**, S. Moulik, "ETA-HP: An Energy and Temperature-Aware Real-time Scheduler for Heterogeneous Platforms"- *The Journal of Supercomputing, Springer **[SUPE]*** Vol. 78, Article 8, May 2022.
- **S. Chakraborty**, S. Saha, M. Själander, and K. D. McDonald-Maier, "Prepare: Power-Aware Approximate Real-time Task Scheduling for Energy-Adaptive QoS Maximization"- *ACM Transactions on Embedded Computing Systems **[TECS]***, Vol. 20, Issue 5s, Article 62, October 2021, 25 Pages.
- **S. Chakraborty**, and M. Själander, "WaFFLe: Gated Cache-Ways with Per-core Fine-grained DVFS for Reduced On-chip Temperature and Leakage Consumption", *ACM Transactions on Architecture and Code Optimization **[TACO]***, Vol. 18, Issue 4, Article 55, December 2021, 25 pages.
- S. Moulik, Z. Das, Rajesh D., and **S. Chakraborty**, "SEAMERS: A Semi-partitioned Energy-Aware scheduler for heterogeneous MulticorE Real-time Systems." *Journal of Systems Architecture (ScienceDirect) **[JSA]***, Vol. 114, Article 101969, March 2021.

- **S. Chakraborty**, and H. K. Kapoor, "Exploring the Role of Large Centralised Caches in Thermal Efficient Chip Design." *ACM Trans. Des. Autom. Electron. Syst. **[TODAES]***, Vol. 24, Issue 5, Article 52, June 2019, 28 pages.
- **S. Chakraborty**, and H. K. Kapoor, "Analysing the Role of Last Level Caches in Controlling Chip Temperature", *IEEE Transactions on Sustainable Computing **[TSUSC]***, Vol. 3, No. 4, Oct.-Dec. 2018, Pages 289-305.
- **S. Chakraborty**, and H. K. Kapoor, "Performance linked Dynamic Cache Tuning: A Static Energy Reduction Approach in Tiled CMPs", *Journal of Microprocessors and Microsystems (Elsevier) **[MICPRO]***, Volume 52, July 2017, Pages 221-235.

Conferences

- **S. Chakraborty**, V. Soteriou, M. Själander, "STIFF: Thermally Safe Temperature Effect Inversion Aware FinFET based Multi-core"-*19th ACM International Conference on Computing Frontiers **(CF 2022)**, 2022.*
- Y. Sharma, S. Moulik and **S. Chakraborty**, "RESTORE: Real-Time Task scheduling on a Temperature Aware FinFET based Multicore"-*Design, Automation & Test in Europe Conference & Exhibition **(DATE 2022)**, 2022.*
- S. Agarwal, and **S. Chakraborty**, "ABACa: Access Based Allocation on Set Wise Multi-Retention in STT-RAM Last Level Cache"-*The 32nd IEEE International Conference on Application-specific Systems, Architectures and Processors **(ASAP 2021)**, 2021.*
- **S. Chakraborty**, S. Saha, M. Själander, and K. D. McDonald-Maier, "RePAiR: A Strategy for Reducing Peak Temperature while Maximising Accuracy of Approximate Real-Time Computing: Work-in-Progress"-*In Proceedings of the International Conference on Hardware/Software Codesign and System Synthesis Companion **(IEEE/ACM CODES + ISSS '20)**, 2020.*
- A. A. Kulkarni, **S. Chakraborty**, S. P. Mahajan, and H. K. Kapoor, "Utility Aware Snoozy Caches for Energy Efficient Chip Multi-Processors"-*ACM Great Lakes Symposium on VLSI **(GLSVLSI)**, 2018*, Chicago, Illinois, USA.
- **S. Chakraborty**, and H. K. Kapoor, "Towards Controlling Chip Temperature by Dynamic Cache Reconfiguration in Multiprocessors"-*30th International Conference on VLSI Design **(VLSID)***, 2017, pp. 75-80, Hyderabad, India.
- **S. Chakraborty**, and H. K. Kapoor, "Static Energy Reduction by Performance Linked Dynamic Cache Resizing"-*IFIP/IEEE International Conference on Very Large Scale Integration **(VLSI-SoC '16)***, 2016, pp. 1-6, Tallinn, Estonia.
- **S. Chakraborty**, S. Das and H. K. Kapoor, "Static Energy Efficient Cache Reconfiguration for Dynamic NUCA in Tiled CMPs"-*Proceedings of the 31st Annual ACM Symposium on Applied Computing **(SAC '16)***, 2016, pp. 1739–1744, Pisa, Italy.
- H. K. Kapoor, S. Das and **S. Chakraborty**, "Static energy reduction by performance linked cache capacity management in Tiled CMPs"-*Proceedings of the 30th Annual ACM Symposium on Applied Computing **(SAC '15)***, 2015, pp. 1913–1918, Salamanca, Spain.
- **S. Chakraborty**, S. Das and H. K. Kapoor, "Performance constrained static energy reduction using way-sharing target-banks", *IEEE International Parallel and Distributed Processing Symposium Workshop **(IPDPSW '15)***, 2015, pp. 444-453, Hyderabad, India.
- **S. Chakraborty**, S. Das and H. K. Kapoor, "Power Aware Cache Miss Reduction by Energy Efficient Victim Retention"- *19th International Symposium on VLSI Design and Test **(VDAT '15)***, 2015, pp. 1-6, Ahmedabad, India.
- N. K. Meena, H. K. Kapoor, and **S. Chakraborty**, "A New Recursive Partitioning Multicast Routing Algorithm for 3D Network-on-Chip". *18th International Symposium on VLSI Design and Test **(VDAT '14)***, 2014, pp. 1-6, Coimbatore, India.

PhD Forum (Poster Presentation)

- VLSI Design 2017, VLSI-SoC 2016

Google Scholar Index

- h-index: 6, i10-index: 3, citations: 94, according to Google Scholar as of 30-Dec-2022. (Link to Google Scholar *Profile: https://scholar.google.com/citations?user=51knrLIAAAAJ&hl=en*)

Professional Membership ACM Member, IEEE Senior member

Skill Set

- **Programming Languages:** JAVA, C++, C, Python
- **Hardware Simulators:** CACTI, Simics, GEMS, HotSpot, Multi2Sim, McPAT, NVSim, DESTINY, Gem5
- **Mathematical Tools:** MATLAB, PRISM, MAPLE

References

- Prof. Magnus Själander,
  Dept. of Computer Science,
  IT Bygget, NTNU, Høgskoleringen 1, Trondheim 7491, Norway.
  Ph.: +47-7359-3682
  E-mail: magnus.sjalander@ntnu.no
- Prof. Hemangee K. Kapoor,
  Dept. of Computer Science & Engineering (CSE),
  IIT Guwahati, Guwahati-781039 (Assam), India.
  Ph.: +91-361-2582363
  E-mail: hemangee@iitg.ac.in
- Prof. Klaus McDonald-Maier,
  School of Computer Science and Electronic Engineering (CSEE),
  University of Essex, 1NW.4.22, Colchester Campus, UK.
  Ph.: +44 (0) 1206 874376
  E-mail: kdm@essex.ac.uk

Declaration I do hereby declare that the particulars of information and facts stated herein above are true, correct and complete to the best of my knowledge and belief.

Date: 01-Jan-2023
Place: Trondheim, Norway

Signature
(SHOUNAK CHAKRABORTY)