DI LIU

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POSITION

Associate Professor, Department of Computer Science, Norwegian University of Technology and Science (NTNU)

EDUCATION

Ph.D in Computer Science, Leiden University, The Netherlands 2011-2017
D Liu. "Latency, energy, and schedulability of real-time embedded systems". PhD thesis. Leiden University, 2017.

M.Eng in Electronic Engineering , Northwestern Polytechnical University, China 2008 - 2011
Major: Signal and information processing

B.Eng in Electronic Engineering , Northwestern Polytechnical University, China 2008 - 2011
Major: Electronic and Information Engineering

EXPERIENCE

Associate Professor Dec 2022 - Present
Department of Computer Science, Norwegian University of Science and Technology *Trondheim, Norway*

Research Fellow Jan 2020 - Jan 2022
HP-NTU Corporate Lab, Nanyang Technological University *Singapore*

Assistant Professor Apr 2018 - Nov 2022
School of Software, Yunnan University *Kunming, China*

Research Assistant Nov 2016 - Apr 2017
Department of Computing, The Hong Kong Polytechnic University *Hong Kong, China*

REWARDS

Best Paper Nominee of CODES-ISSS, 2015
Donglu Young Fellowship of Yunnan University, 2019
Yunnan Young Talented Program, 2019
Publicity Paper of DAC, 2022

RESEARCH GRANTS

Mixed-criticality systems on heterogeneous multicore systems, Young Scholar, National Natural Science Foundation of China, Grant No. 61902341, 250,000 RMB, 2020-2022, PI

Edge Processor Evaluation, co-funded by National Research Foundation (NRF) Industry Alignment Fund - Industry Collaboration Projects (IAF-ICP), Singapore and HP Inc. at Palo Alto, US, co-founded the HP-NTU Digital Manufacturing Corporate Lab, SGD 3,500,000, 2018-2022, main participator

Research on the key technologies of cooperative communications base on the user trust degree, National Natural Science Foundation of China, Grant No. 61801418, 250,000 RMB, 2019-2021, main participator

PUBLICATIONS

Peer-Reviewed Conferences

[1] **Liu, D.**, J. Spasic, J. T. Zhai, T. Stefanov, and G. Chen. "Resource optimization for csdf-modeled streaming applications with latency constraints". In: *2014 Design, Automation & Test in Europe Conference & Exhibition (DATE)*. IEEE. 2014, pp. 1–6.

[2] Chen, G., B. Hu, K. Huang, A. Knoll, and **D. Liu**. "Shared l2 cache management in multicore real-time system". In: *2014 IEEE 22nd Annual International Symposium on Field-Programmable Custom Computing Machines*. IEEE. 2014, pp. 170–170.

[3] Chen, G., B. Hu, K. Huang, A. Knoll, **D. Liu**, and T. Stefanov. "Automatic cache partitioning and time-triggered scheduling for real-time MPSoCs". In: *2014 International Conference on ReConFigurable Computing and FPGAs (ReConFig14)*. IEEE. 2014, pp. 1–8.

[4] Spasic, J., **D. Liu**, E. Cannella, and T. Stefanov. "Improved hard real-time scheduling of CSDF-modeled streaming applications". In: *2015 International Conference on Hardware/Software Codesign and System Synthesis (CODES+ ISSS)*. IEEE. 2015, pp. 65–74.

[5] **Liu, D.**, J. Spasic, G. Chen, and T. Stefanov. "Energy-efficient mapping of real-time streaming applications on cluster heterogeneous mpsocs". In: *2015 13th IEEE symposium on embedded systems for real-time multimedia (ESTIMedia)*. IEEE. 2015, pp. 1–10.

[6] **Liu, D.**, J. Spasic, N. Guan, G. Chen, S. Liu, T. Stefanov, and W. Yi. "EDF-VD scheduling of mixed-criticality systems with degraded quality guarantees". In: *2016 IEEE Real-Time Systems Symposium (RTSS)*. IEEE. 2016, pp. 35–46.

[7] Spasic, J., **D. Liu**, and T. Stefanov. "Exploiting resource-constrained parallelism in hard real-time streaming applications". In: *2016 Design, Automation & Test in Europe Conference & Exhibition (DATE)*. IEEE. 2016, pp. 954–959.

[8] **Liu, D.**, J. Spasic, P. Wang, and T. Stefanov. "Energy-efficient scheduling of real-time tasks on heterogeneous multicores using task splitting". In: *2016 IEEE 22nd International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA)*. IEEE. 2016, pp. 149–158.

[9] Spasic, J., **D. Liu**, and T. Stefanov. "Energy-efficient mapping of real-time applications on heterogeneous MPSoCs using task replication". In: *Proceedings of the Eleventh IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis*. 2016, pp. 1–10.

[10] Jiang, X., N. Guan, **D. Liu**, and W. Liu. "Analyzing GEDF Scheduling for Parallel Real-Time Tasks with Arbitrary Deadlines". In: *Design, Automation & Test in Europe Conference & Exhibition*. 2019.

[11] Guo, Z., A. Bhuiyan, **D. Liu**, A. Khan, A. Saifullah, and N. Guan. "Energy-Efficient Real-Time Scheduling of DAGs on Clustered Multi-Core Platforms". In: *2019 IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS)*. 2019.

[12] Yu, J.-J., M. Zhao, W.-T. Li, **D. Liu**, S. Yao, and W. Feng. "Joint offloading and resource allocation for time-sensitive multi-access edge computing network". In: *2020 IEEE Wireless Communications and Networking Conference (WCNC)*. IEEE. 2020, pp. 1–6.

[13] Luo, X., **D. Liu**, H. Kong, and W. Liu. "Edgenas: Discovering efficient neural architectures for edge systems". In: *2020 IEEE 38th International Conference on Computer Design (ICCD)*. IEEE. 2020, pp. 288–295.

[14] Luo, X., **D. Liu**, S. Huai, and W. Liu. "Hsconas: Hardware-software co-design of efficient dnns via neural architecture search". In: *2021 Design, Automation & Test in Europe Conference & Exhibition (DATE)*. IEEE. 2021, pp. 418–421.

[15] Chen, P., H. Chen, J. Zhou, **D. Liu**, S. Li, W. Liu, W. Chang, and N. Guan. "Partial order based non-preemptive communication scheduling towards real-time networks-on-chip". In: *Proceedings of the 36th Annual ACM Symposium on Applied Computing*. 2021, pp. 145–154.

[16] Huai, S., L. Zhang, **D. Liu**, W. Liu, and R. Subramaniam. "Zerobn: Learning compact neural networks for latency-critical edge systems". In: *2021 58th ACM/IEEE Design Automation Conference (DAC)*. IEEE. 2021, pp. 151–156.

[17] He, Z., Y. Sun, H. Fang, Y.-X. Huang, Y. Yang, Z.-Y. Zhang, and **D. Liu**. "Energy-Efficient System Design of Asymmetric Multiprocessor for Real-Time Streaming Applications". In: *2021 International Conference on Intelligent Technology and Embedded Systems (ICITES)*. IEEE. 2021, pp. 44–51.

[18] Li, S., **D. Liu**, and W. Liu. "Optimized Data Reuse via Reordering for Sparse Matrix-Vector Multiplication on FPGAs". In: *2021 IEEE/ACM International Conference On Computer Aided Design (ICCAD)*. IEEE. 2021, pp. 1–9.

[19] Kong, H., **D. Liu**, X. Luo, W. Liu, and R. Subramaniam. "HACScale: Hardware-Aware Compound Scaling for Resource-Efficient DNNs". In: *2022 27th Asia and South Pacific Design Automation Conference (ASP-DAC)*. IEEE. 2022, pp. 708–713.

[20] Wang, Z.-H., Z. He, H. Fang, Y.-X. Huang, Y. Sun, Y. Yang, Z.-Y. Zhang, and **D. Liu**. "Efficient On-Device Incremental Learning by Weight Freezing". In: *2022 27th Asia and South Pacific Design Automation Conference (ASP-DAC)*. IEEE. 2022, pp. 538–543.

[21] Yang, Y., **D. Liu**, H. Fang, Y.-X. Huang, Y. Sun, and Z.-Y. Zhang. "Once for all skip: efficient adaptive deep neural networks". In: *2022 Design, Automation & Test in Europe Conference & Exhibition (DATE)*. IEEE. 2022, pp. 568–571.

[22] Luo, X., **D. Liu**, H. Kong, S. Huai, H. Chen, and W. Liu. "You only search once: On lightweight differentiable architecture search for resource-constrained embedded platforms". In: *Proceedings of the 59th ACM/IEEE Design Automation Conference*. 2022, pp. 475–480.

[23] Luo, X., **D. Liu**, H. Kong, S. Huai, H. Chen, and W. Liu. "Work-in-Progress: What to Expect of Early Training Statistics? An Investigation on Hardware-Aware Neural Architecture Search". In: *2022 International Conference on Hardware/Software Codesign and System Synthesis (CODES+ ISSS)*. IEEE. 2022, pp. 1–2.

[24] Huai, S., **D. Liu**, H. Kong, X. Luo, W. Liu, R. Subramaniam, C. Makaya, and Q. Lin. "Collate: Collaborative Neural Network Learning for Latency-Critical Edge Systems". In: *2022 IEEE 40th International Conference on Computer Design (ICCD)*. IEEE. 2022, pp. 627–634.

[25] Kong, H., **D. Liu**, S. Huai, X. Luo, W. Liu, R. Subramaniam, C. Makaya, and Q. Lin. "Smart Scissor: Coupling Spatial Redundancy Reduction and CNN Compression for Embedded Hardware". In: *Proceedings of the 41st IEEE/ACM International Conference on Computer-Aided Design*. 2022, pp. 1–9.

[26] Chen, H., **D. Liu**, S. Li, S. Huai, X. Luo, and W. Liu. "MUGNoC: A Software-configured Multicast-Unicast-Gather NoC for Accelerating CNN Dataflows". In: *Proceedings of the 28th Asia and South Pacific Design Automation Conference*. 2023, pp. 308–313.

[27] Huai, S., **D. Liu**, X. Luo, H. Chen, W. Liu, and R. Subramaniam. "Crossbar-Aligned & Integer-Only Neural Network Compression for Efficient In-Memory Acceleration". In: *Proceedings of the 28th Asia and South Pacific Design Automation Conference*. 2023, pp. 234–239.

Journals

[28] Chen, G., B. Hu, K. Huang, A. Knoll, **D. Liu**, T. Stefanov, and F. Li. "Reconfigurable cache for real-time MPSoCs: Scheduling and implementation". In: *Microprocessors and Microsystems* 42 (2016), pp. 200–214.

[29] Spasic, J., **D. Liu**, E. Cannella, and T. Stefanov. "On the improved hard real-time scheduling of cyclo-static dataflow". In: *ACM Transactions on Embedded Computing Systems (TECS)* 15.4 (2016), pp. 1–26.

[30] Chen, G., N. Guan, **D. Liu**, Q. He, K. Huang, T. Stefanov, and W. Yi. "Utilization-based scheduling of flexible mixed-criticality real-time tasks". In: *IEEE Transactions on Computers* 67.4 (2017), pp. 543–558.

[31] **Liu, D.**, N. Guan, J. Spasic, G. Chen, S. Liu, T. Stefanov, and W. Yi. "Scheduling analysis of imprecise mixed-criticality real-time tasks". In: *IEEE Transactions on Computers* 67.7 (2018), pp. 975–991.

[32] Zhang, D., M. Cui, Y. Yang, P. Yang, C. Xie, **D. Liu**, B. Yu, and Z. Chen. "Knowledge Graph-Based Image Classification Refinement". In: *IEEE Access* 7 (2019), pp. 57678–57690.

[33] Mo, Q., F. Dai, **D. Liu**, J. Qin, Z. Xie, and T. Li. "Development of Private Processes: A Refinement Approach". In: *IEEE Access* 7 (2018), pp. 2169–3536.

[34] Zhao, M., **D. Liu**, H. Gao, and W. Feng. "Confidential Cooperative Communication with the Trust Degree of Jammer". In: *Entropy* 21.6 (2019).

[35] Xue, G., **D. Liu**, J. Liu, and S. Yao. "A process partitioning technique for constructing decentralized web service compositions". In: *Software: Practice and Experience* 49.10 (2019), pp. 1550–1570.

[36] Zhao, M., H. Wang, J. Guo, **D. Liu**, C. Xie, Q. Liu, and Z. Cheng. "Construction of an industrial knowledge graph for unstructured chinese text learning". In: *Applied Sciences* 9.13 (2019), p. 2720.

[37] Wang, K., X. Jiang, N. Guan, **D. Liu**, W. Liu, and Q. Deng. "Real-time scheduling of DAG tasks with arbitrary deadlines". In: *ACM Transactions on Design Automation of Electronic Systems (TODAES)* 24.6 (2019), pp. 1–22.

[38] Zhao, M., **D. Liu**, X. Jiang, W. Liu, G. Xue, C. Xie, Y. Yang, and Z. Guo. "CASS: Criticality-Aware Standby-Sparing for real-time systems". In: *Journal of Systems Architecture* 100 (2019), p. 101661.

[39] Bhuiyan, A., **D. Liu**, A. Khan, A. Saifullah, N. Guan, and Z. Guo. "Energy-efficient parallel real-time scheduling on clustered multi-core". In: *IEEE Transactions on Parallel and Distributed Systems* 31.9 (2020), pp. 2097–2111.

[40] Li, W.-T., M. Zhao, Y.-H. Wu, J.-J. Yu, L.-Y. Bao, H. Yang, and **D. Liu**. "Collaborative offloading for UAV-enabled time-sensitive MEC networks". In: *EURASIP Journal on Wireless Communications and Networking* 2021 (2021), pp. 1–17.

[41] **Liu, D.**, H. Kong, X. Luo, W. Liu, and R. Subramaniam. "Bringing AI to edge: From deep learning's perspective". In: *Neurocomputing* 485 (2022), pp. 297–320.

[42] Xue, G., S. Deng, **D. Liu**, and Z. Yan. "Reaching consensus in decentralized coordination of distributed microservices". In: *Computer Networks* 187 (2021), p. 107786.

[43] **Liu, D.**, S.-G. Yang, Z. He, M. Zhao, and W. Liu. "CARTAD: Compiler-Assisted Reinforcement Learning for Thermal-Aware Task Scheduling and DVFS on Multicores". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 41.6 (2021), pp. 1813–1826.

[44] Zhao, M., W. Li, L. Bao, J. Luo, Z. He, and **D. Liu**. "Fairness-aware task scheduling and resource allocation in UAV-enabled mobile edge computing networks". In: *IEEE Transactions on Green Communications and Networking* 5.4 (2021), pp. 2174–2187.

[45] Kong, H., S. Huai, **D. Liu**, L. Zhang, H. Chen, S. Zhu, S. Li, W. Liu, M. Rastogi, R. Subramaniam, et al. "EDLAB: A benchmark for edge deep learning accelerators". In: *IEEE Design and Test* (2021).

[46] Luo, X., **D. Liu**, S. Huai, H. Kong, H. Chen, and W. Liu. "Designing Efficient DNNs via Hardware-Aware Neural Architecture Search and Beyond". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 41.6 (2021), pp. 1799–1812.

[47] Zhao, M., J.-J. Yu, W.-T. Li, **D. Liu**, S. Yao, W. Feng, C. She, and T. Q. Quek. "Energy-aware task offloading and resource allocation for time-sensitive services in mobile edge computing systems". In: *IEEE Transactions on Vehicular Technology* 70.10 (2021), pp. 10925–10940.

[48] Yang, S.-G., Y.-Y. Wang, W. Liu, X. Jiang, M. Zhao, H. Fang, Y. Yang, and **D. Liu**. "Temperature-aware Task Scheduling on Multicores Based on Reinforcement Learning". In: *Journal of Software* 32.8 (2021), pp. 2408–2424.

[49] Pang, W., X. Jiang, M. Lv, T. Gao, **D. Liu**, and W. Yi. "Toward the Predictability of Dynamic Real-Time DNN Inference". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 41.9 (2021), pp. 2849–2862.

[50] Zhu, S., L. H. Duong, H. Chen, **D. Liu**, and W. Liu. "FAT: An In-Memory Accelerator with Fast Addition for Ternary Weight Neural Networks". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (2022).

[51] Jiang, W., Z. Song, J. Zhan, **D. Liu**, and J. Wan. "Layerwise Security Protection for Deep Neural Networks in Industrial Cyber Physical Systems". In: *IEEE Transactions on Industrial Informatics* 18.12 (2022), pp. 8797–8806.

[52] Luo, X., **D. Liu**, H. Kong, S. Huai, H. Chen, and W. Liu. "SurgeNAS: A Comprehensive Surgery on Hardware-Aware Differentiable Neural Architecture Search". In: *IEEE Transactions on Computers* (2022).

[53] Huai, S., **D. Liu**, H. Kong, W. Liu, R. Subramaniam, C. Makaya, and Q. Lin. "Latency-constrained DNN architecture learning for edge systems using zerorized batch normalization". In: *Future Generation Computer Systems* 142 (2023), pp. 314–327.

[54] Luo, X., **D. Liu**, H. Kong, S. Huai, H. Chen, and W. Liu. "Lightnas: On lightweight and scalable neural architecture search for embedded platforms". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (2022).

TEACHING

Teaching activities at Norwegian University of Science and Technology, course coordinator

- TDT4186 Operating Systems (2023)

Teaching activities at Yunnan University, solo instructor

- Introduction to Operating Systems (2018, Chinese)
- Research Seminar (2018, 2019, Chinese)

- Digital Circuit (2018,2019, Chinese)
- Advanced Topics Seminar (2018, 2019, Chinese)
- Introduction to Programming (2018, English for international students)
- Computer Architectures and Organization (2019, English for international students)

PROFESSIONAL SERVICES

Editorship

- Guest Editor, Special Issue on the 2019 IEEE Symposium on Real-Time Computing ISORC, Journal of Systems Architectures

Involvement in conferences

- PC member, Artificial Evaluation, IEEE Real-Time and Embedded Technology (RTAS), 2023
- Special Session Chair, International Conference on Intelligent Technology and Embedded Systems (ICITES) 2021, 2022
- PC member, poster/demo co-chair, IEEE International Symposium on Real-Time Computing (ISORC) 2019
- PC member, China Computer Federation Symposium on Dependable Software Engineering (SETTA) 2019
- PC member, China Computer Federation Embedded Systems Technology Conference (ESTC) 2019

Reviewer or Secondary Reviewer:

- IEEE Symposium on Embedded Systems for Real-Time Multimedia
- International Conference Design, Automation and Test in Europe
- IEEE/ACM Conference on HW/SW Codesign and System Synthesis
- International Workshop on Software and Compilers for Embedded Systems
- ACM Transactions on Design Automation of Electronic Systems
- Journal of Circuits, Systems, and Computers
- IEEE Transaction on Computers
- Desgin Automation Conference
- Asia and South Pacific Design Automation Conference
- IEEE Real-Time and Embedded Technology and Applications Symposium
- Euromicro Conference on Real-Time Systems
- Journal of Systems Architectures (JSA)
- IEEE ACCESS
- IEEE Transactions on Industrial Informatics
- IEEE Transactions on Emerging Topics in Computing
- IEEE Internet of Things Magazine
- World Wide Web Journal
- Digital Communications and Networks
- Software: Practice and Experience
- IEEE Real Time Systems Symposium
- IEEE International Conference On Computer Aided Design